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An MWIR payload with FPGA-based data processing for a 12U nanosatellite

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Abstract: In this paper, we describe an infrared imaging payload for a 12U nanosatellite. It contains a cryocooled MWIR detector and FPGA-based data processing unit. The system performs background monitoring in spectral bands with low atmospheric transmission. At the core of the system, a modern FPGA System-on-chip provides the computational performance, interfaces and mass storage for capturing, processing and storing high-resolution images. While the payloads mass of 2.5 kg and power requirements of 17 W exceed the capabilities of the common 2-3U CubeSats, it brings a level of performance to the increasingly popular 12U form factor that was previously reserved for much larger systems.

1. INTRODUCTION

Fraunhofer EMI currently designs, builds and tests an MWIR (Mid-Wavelength Infrared) payload for a 12U nanosatellite. The mission is called ERNST (Experimental Spacecraft based on Nanosatellite Technology) and its main goal is to evaluate the utility of a nanosatellite mission for scientific and military purposes. The satellite bus is based on CubeSat components where possible and its main payload is an advanced MWIR camera. The system performs background monitoring in spectral bands with low atmospheric transmission which have not yet been extensively characterized.

2. MWIR PAYLOAD SYSTEM

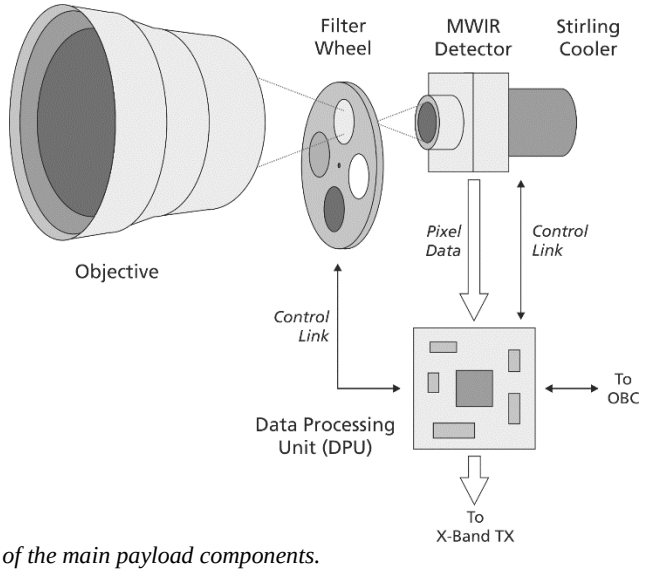

Figure 1: Block diagram of the main payload components.

The payload consists of a commercially available infrared lens, a custom designed filter wheel for switching between multiple spectral bands and the infrared detector unit. The detector unit comprises a 1.3 Megapixel InSb sensor with a spectral range of 3-5 µm and a digital ROIC (Readout Integrated Circuit). It provides the raw image data via a digital serial high-speed interface. The detector is actively cooled by a rotary Stirling cryocooler to an operating temperature of 77 K. This cooler posed one of the biggest challenges during the payload design, as it generates substantial heat and vibrations. Both effects have been carefully analyzed and an optimized structure has been found that allows the continuous operation of the cooler without negative effects on the image quality.

Attached to the hot end of the cooler is a 3D structured radiator that allows efficient heat irradiation. The radiator is manufactured using Additive Manufacturing technology ("3D-printing"), specifically the Selective laser melting (SLM) process.

Depending on the operation mode of the Data Processing Unit, the payload consumes up to 17 W of power. The largest part of the energy budget is the cooler, which consumes 9 W at its operating temperature and up to 18 W when cooling down from ambient temperature. These rather high power requirements have major influence on the design of the nanosatellite platform and especially its power subsystem. One consequence is that even a 12U platform needs deployable solar panels to provide enough power for continuous operation. The whole payload has the volume of approximately 3 CubeSat units and weighs about 2.5 kg.

The expected performance of the payload is up to 150 m GSD (Ground Sample Distance) at a 700 km sun-synchronous orbit and a swath width of around 200 km. The optics have been optimized for a large swath width rather than the highest ground resolution. The system is currently being integrated at Fraunhofer EMI and will be available as an engineering model by the end of 2017. Subsequently, thermal vacuum, vibration, and radiation testing will be performed further pursuing space qualification.

3. DATA PROCESSING UNIT

A so-called Data Processing Unit (DPU) handles the processing and storage of the captured image data as well as the controlling of the payload's subsystems. The system described here can be seen as a successor to the DPU currently flying on the Kent Ridge 1 microsatellite [1]. The main difference to the previous system is the use of an SoC combining an FPGA and a powerful CPU instead of using just an ARM processor. This is a very attractive choice as the tight coupling of on-chip high-speed buses with both the FPGA and CPU allows for very efficient interwork between natively executed software in the processor and IP modules in the programmable logic part.

Figure 2 shows a block diagram of the major functional components of the DPU.

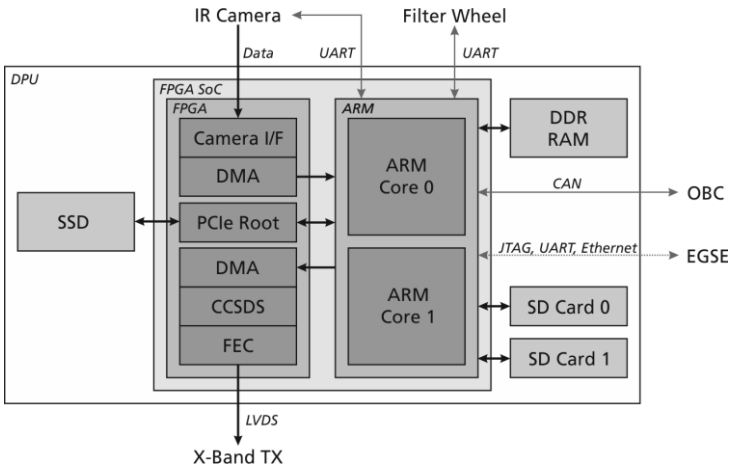

Figure 2: Block diagram of the DPU hardware platform. Logic cores inside the programmable area of the FPGA SoC are included in the diagram.

3.1 DPU Hardware

Since designing a custom PCB with an FPGA SoC is a major effort, we chose a so-called System on Module (SoM) that complements the main SoC with all required peripherals like DDR RAM, flash memory and power supply circuits on a small PCB. The SoM sits on top of a custom baseboard that complies with the CubeSat standard. Besides the simplification of the hardware development, this concept allows us to switch between different FPGA SoCs with no or minimal changes to the custom baseboard. Currently, we are using an SoC from the Zynq-7000 Series by Xilinx [2]. With the SoM concept, we could switch to the upcoming Zynq UltraScale+ MPSoC [3] without having to design a new FPGA board. This step promises even higher processing and interfacing capabilities than the current solution.

The baseboard as shown in Figure 3 contains mainly connectors for the different interfaces and only some basic peripheral circuits. For mass storage, the baseboard is also equipped with a COTS solid state disk (SSD) attached via PCI Express (PCIe) and two independent micro SD flash storage cards.

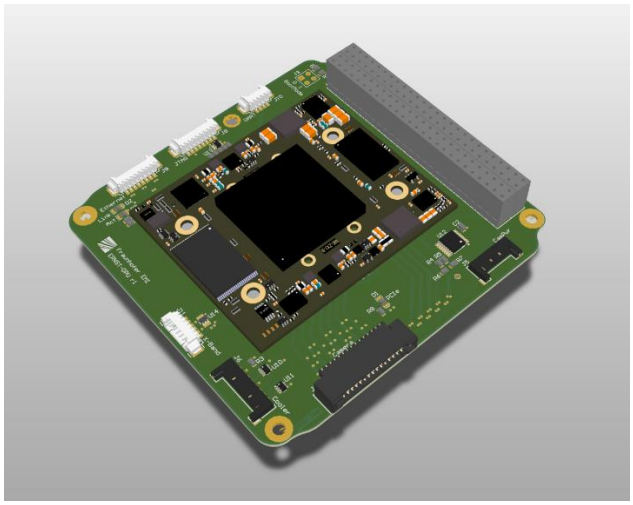

Figure 3: Rendered view of the DPU hardware platform. The FPGA-SoM sits on top of the CubeSat baseboard. The PCIe SSD and the microSD cards are mounted on the rear side of the board.

The programmable logic part of the FPGA SoC fulfills multiple tasks. The first is to provide all non-standard hardware interfaces to the CPU. We use custom IP cores to implement the performance sensitive interfaces to the MWIR detector and the X-Band transmitter. Both interfaces are high-speed serial LVDS (Low Voltage Differential Signalling) links for which we take advantage of the integrated SerDes blocks of the FPGA. The CPU can access the two interfaces using DMA (Direct Memory Access) since they are mapped to the processor's address space.

Secondly, the FPGA implements computationally intensive algorithms to reduce the CPU load. Currently, this is primarily the CCSDS protocol stack ([4–6]) including Reed Solomon Forward Error Correction (FEC). In later stages of the development, we plan to move image-processing algorithms from the processor to the FPGA as well.

Thirdly, the programmable logic provides the PCIe interface to the mass storage device. Using the shared internal high-speed bus between the CPU and the FPGA inside the SoC it is possible to achieve high data throughput rates.

Finally, the FPGA contains several peripheral logic blocks. For example, the infrared detector needs a frame sync signal with specific timing requirements. This signal is generated by a custom logic block that can be controlled from the processor.

3.2 DPU Software

The DPU's software is based on an embedded Linux operating system. This way we can benefit from a well-tested, documented, and standards-compliant software environment. The Linux kernel already includes many necessary hardware drivers, for example for storage, file systems, and peripheral busses like CAN, UART and I^2C. To interface with the hardware modules in the FPGA described above, we implemented several custom kernel drivers. All mission specific software is executed in user space allowing tight monitoring, rapid restarts and reasonable abstraction of the hardware layer.

The mission software performs all image processing that is required for infrared imaging. This includes everything from bad pixel replacement and non-uniformity correction to lossless image compression. Furthermore, the software is responsible for managing the acquired data in the different storage media. Finally, the DPU software controls the detector and the filter wheel and is able to provide a CCSDS conforming data stream for downlink with utilization of the aforementioned logic blocks.

4. CONCLUSION

In this work, we present an advanced mid-wave infrared payload for a 12U nanosatellite. Its design philosophy is to use commercially available parts and systems as much as possible. We only add specialized custom parts where COTS solutions are not available or where they allow for significant enhancements.

A highly integrated FPGA SoC acts as the central control and data processing unit for the payload. It provides all functionality from image acquisition and processing to storage management and a CCSDS protocol stack for data downlink.

Compared to the imaging payloads that is usually found on nanosatellites and CubeSats, the system described here provides unmatched performance. Especially the MWIR spectral band that requires a cooled detector leads to demanding requirements for the satellite bus. In the ERNST mission, we will demonstrate that these requirements can be met with a 12U nanosatellite.

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