SOLAR MINI MODULE MADE WITH EPITAXIAL CRYSTALLINE SILICON THIN-FILM WAFER EQUIVALENTS

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ABSTRACT: Crystalline silicon thin-film solar cells manufactured at high temperature are capable to be processed using standard wafer processes. However the proof of this claim was still missing for stringing and encapsulation of those cells to a module. It was the intention of the work reported in this paper to show the validity of this claim. We manufactured large-area solar cells in epitaxial layers on highly doped Cz and mc-Si substrates (epitaxial wafer equivalents), using various technologies of different complexity. On 143 cm^2 large monocrystalline epitaxial wafer equivalents, we could achieve 15.2% efficiency. Two kinds of cells were interconnected and laminated to mini modules of 368 cm^2 and 576 cm^2 aperture area, respectively. Standard techniques have been successfully applied to manufacture the modules, yielding efficiencies of 12.2% and 10.2%, respectively.

Keywords: Epitaxy - 1: Crystalline Silicon Films - 2: Module Manufacturing- 3

1 INTRODUCTION

The high-temperature approach for crystalline silicon thin-film (CSiTF) solar cells [1] is one promising option for realizing a cost effective alternative to today's wafer solar cells. A major advantage of the Si layers made in this approach is their compatibility to the temperatures applied in standard wafer processing, since the temperatures applied in their manufacturing usually is well beyond 1200 K. If in addition the substrate/layer structure can be processed to a solar cell using exactly the same process like used for a Si wafer, we call it "wafer equivalent". There are several possibilities to realize wafer equivalents, all of them unite the fact that all substrate and layers used are electrically conductive, hence both side contacting is applicable. The most simple type of wafer equivalent is the so-called epitaxial wafer equivalent: it solely consists of a usually highly doped c-Si substrate with a thin epitaxial silicon layer deposited on it, the latter serving as active solar cell absorber. Solar cells from epitaxial wafer equivalents on various kinds of c-Si substrates have been processed by several institutes with varying cell processes and cell areas ranging from 4 cm^2 to 100 cm^2 (see e.g. [2], [3]). Efficiencies up to 17.6% have been reported using high-efficiency cell processes [4], 13.8% using production-type screen printing processes [5].

The work described in this paper had two purposes: first, applicability of a standard cell process to an epitaxial wafer equivalent featuring cell sizes close to standard wafer size should be shown. Second, it should be tested if such solar cells could be interconnected and encapsulated using a standard module processing, however on a small module size in the order of approx. 500 cm^2 aperture area.

2 SOLAR CELL AND MODULE FABRICATION

2.1 Sample structure

Fig. 1 illustrates the sample structure realized for the work reported here. It consists of an electrically inactive p+ Si substrate, on which two epi layers were deposited in-situ. The first, highly doped epi layer not only serves as a back surface field generating layer, but also separates the growth interface from the second layer, which is lowly doped and therefore acts as electrically active layer. Junction diffusion, metallization and antireflection coating can be applied as for a standard wafer.

Two different kinds of substrates were used:

- polished, highly boron doped (~$5 \cdot 10^{18}$ cm^{-3}) prime-grade 6" Cz wafer of approx. 700 µm thickness
- highly boron doped (~3e18 at/cm^3) cast 100x100 mm^2 mc-Si wafers of approx. 330 µm thickness

Prior to epitaxy, saw damage was removed on the mc-Si wafers by CP133 followed by a standard RCA cleaning etch. By atmospheric pressure CVD in a commercial reactor of a 3rd party company, a low-defect epitaxial layer stack was deposited consisting of a 5µm $1 \cdot 10^{19}$ cm^{-3} BSF layer, and a 35 µm $8 \cdot 10^{16}$ cm^{-3} active layer on both substrate types.

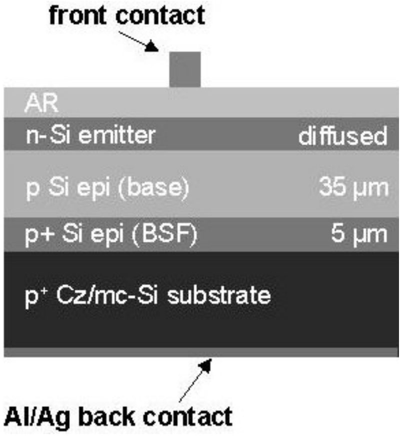

Fig. 1: Sample structure of a solar cell made from an epitaxial wafer equivalent.

2.2 Solar cell fabrication

Three different solar cell processes were applied to the Cz wafer equivalents:

- a high efficiency process (process “A”) on 5” pseudo square, including random pyramid texture, blue sensitive emitter, thick thermal passivation oxide which also acts as antireflection coating and metal contacts made by photolithography followed by evaporation and electroplating.
- a clean room process (process “B”) on 100x100 mm^2, including 120 Ohm/sq. $POCl_3$ diffusion, passivation oxide, evaporation and electroplating of contacts defined by photolithography, single layer TiO_2 AR coating and Al/Ag rear contacts. The thickness of the AR coating was adapted to an encapsulation of the cell in a module.
- a screen printing process (process “C”) on 100x100 mm^2, including 40 Ohm/sq. $POCl_3$ diffusion, PECVD-SiN_x AR coating and screen printed contacts fired through the AR coating.

Only the slightly modified process C was applied to mc-Si wafer equivalents. Instead of PECVD-SiN_x, sputter-deposited SiN_x was used as AR coating. Since the surface of the epitaxial layer is free of crystal damage, no damage etch was necessary prior to the solar cell process.

2.3 Module fabrication

Two modules were manufactured from either Cz (process B) or mc wafer equivalents (process C). The former module consisted of four cells, the latter of six cells. The solar cells were connected in series by soldering copper tabs by hand on the front and on the back side. The contact material was a lead free solder (Sn95,5Ag3,8Cu0,7) with a melting point of 217°C. Due to the thickness of the Cz wafer equivalents, good solder points were very hard to do because the silicon dissipates most of the heating energy. Nevertheless mechanical and electrical stabile contacts have been achieved on both module types. The so prepared solar cell matrix has been laminated between a front glass and a Tedlar® back side foil using three fast cure EVA (ethylene vinyl acetate) sheets. An additional third EVA sheet was used for the Cz based module because of the cell thickness. In this way it could be made sure that enough EVA was in the module to surround all the cells. The additional EVA sheet has been placed behind the cells to keep light absorption at a minimum. The principle structure of the module design is shown in figure 2. The module has been laminated in a small laboratory laminator using our standard lamination process for EVA shown in figure 3. In both module processes, no wafer break occurred.

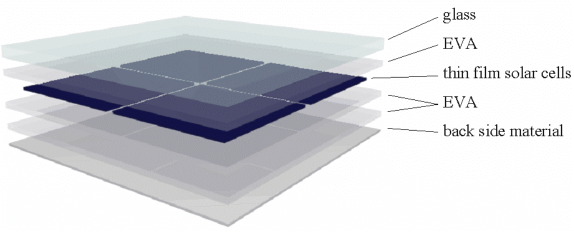

Fig. 2: Principle structure of the CSiTF mini module.

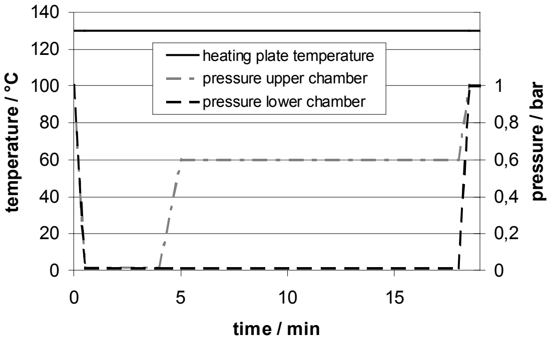

Fig. 3: Standard lamination process for fast cure EVA.

3 RESULTS

3.1 Solar cell results

Table 1 summarizes the mean values of illuminated solar cell parameters achieved for all cell processes described in the previous section. Independent on applied process on Cz substrates, the deviation from mean is always smaller than 2%, reflecting the high reproducibility of the epitaxial deposition process as well as the excellent stability of the cell processes applied. For mc-Si substrates, the applied screen printing process yields in a two fold higher deviation from mean values.

3.1.1 Cells made by process A and B

In spite of their 50% larger area, the cells of process A still are those with the best performance amongst the Cz processes. The values of the best cell were V_{oc}=649.3 mV, I_{sc}=29.4 mA/cm^2, FF=79.7%, η=15.2%. This result can be compared to a 4 cm^2 large cell reported by Faller et. al. [4], who could achieve a 15% relative higher efficiency. Since the difference in performance can be explained by a better solar cell process (e.g. inverted pyramids instead of random pyramids) and a slightly increased layer thickness, the statement seems to be true that on high-quality substrates the area of epitaxial wafer equivalents can be scaled up without losses due to material quality.

The significantly simpler process B, which was designed for cell encapsulation in a module, still resulted in a reasonably high efficiency (best cell: V_{oc}=639 mV, I_{sc}=27.4 mA/cm^2, FF=79.5%, η=13.9%). It is remarkable that V_{oc} of those cells is significantly higher than the V_{oc} of the Cz reference cell, presumably due to lower impurity content of the epi layer, and better passivation of the rear surface. For nearly all cells of process B, the parallel resistance is comparatively low. This might be due to some edge shunting occurred during deposition of the Ag layer of the back contact, which was done without masking, and which maybe was not completely removed after deposition.

The reflectance measurement (see Fig. 2) shows in the low-wavelength region the effect of optimizing the AR coating for encapsulation of the cells: the huge increase of the reflectance between 300 and 500 nm is due to this fact, and is responsible for loss of some current compared to optimized AR layers. The IQE curve reflects very impressively the effect of missing optical confinement: starting from approx. 750 nm, the IQE decreases rapidly, in accordance to the absorption length which is in the order of the active layer thickness of 35 µm. This behaviour clearly demonstrates the need for efficient optical confinement to gain current from the long-wavelength light.

Material/ Process	Area [cm²]	V_{OC} [mV]	J_{SC} [mA/cm²]	FF [%]	η [%]
Cz process A	143,3	648,6 ± 0,7	29,3 ± 0,1	79,1 ± 0,6	15,1 ± 0,1
Cz process B	92,2	638,3 ± 0,7	27,5 ± 0,2	78,6 ± 0,9	13,8 ± 0,1
Cz process C	96,0	616,5 ± 2,2	25,7 ± 0,3	73,2 ± 2,1	11,6 ± 0,2
mc process C	96,0	588,0 ± 2,2	25,0 ± 0,1	73,0 ± 2,3	10,7 ± 0,4

Table 1: Overview of mean illuminated solar cell parameters of all cell processes described in this paper.

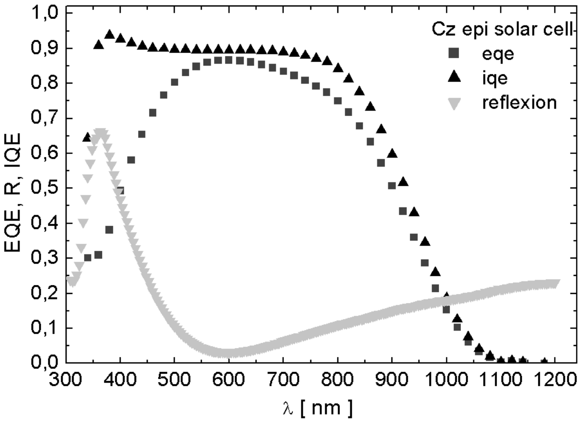

Fig. 4: Internal and external quantum efficiency as well as reflection curves measured at the best Cz CSiTF cell of process B.

3.1.2 Cells made by process C

Due to the high substrate thickness, firing conditions had to be optimized prior to firing the Cz wafer equivalent cells. The comparatively low fill factor however still reflects some small persistent further potential, which could not be clarified by thermography measurements. In spite of this, the cell result of the best cell (V_{oc}=617 mV, I_{sc}=25.5 mA/cm^2, FF=75.3%, η=11.8%) is not too far from our best value on 23 cm^2 cells (η=12.4%) [6].

As for Cz cells of process C, optimum firing conditions had to be found also for the wafer equivalents based on mc-Si substrates. Compared to them, V_{oc} and I_{sc} are significantly lower. One reason for that is presumably the different methods to deposit the AR coating in these two processes: SiN_x on Cz wafer equivalents was deposited hydrogen-rich using PECVD, whereas the sputtered SiN_x on mc-Si substrates had no additional hydrogen source in the process gas. Therefore, both bulk and surface passivation of the mc-Si cells is assumed to be worse than for the mono-Si cells. Nevertheless the absolute value of cell efficiency on mc-Si cells is nearly as high, and the deviation from mean is even better than reported for smaller (23 cm^2) cells using the same cell process as the mono-Si cells [6], revealing again the high quality of the epitaxial layer and the stability of the cell process.

3.2 Module results

3.2.1 Module from monocrystalline CSiTF solar cells

Performance of the CSiTF mini module could only be measured outdoor, since both voltage, current and size of it did not fit to any indoor sun tester. However due to tracking and a nice summer nearly standard conditions could be achieved for measurement: temperature of 28.7°C at an irradiation of 959.5 W/m^2, in Freiburg/Germany. Compared to the parameters of the single cells, the module parameters differed somewhat (see Fig. 5). The module's efficiency was measured to be 12.2% (cell aperture area of 368 cm^2) at these conditions, approx. 11% lower as the mean cell value. The same is true for V_{oc} (module: 2330 mV compared to 2554 mV sum of the single cells) and FF (71.4% vs. ~78.5%). This decrease is presumably due to the difficulties during soldering the tabs described above, yielding in sub-optimal contacts between busbars and tabs and therefore higher series resistance.

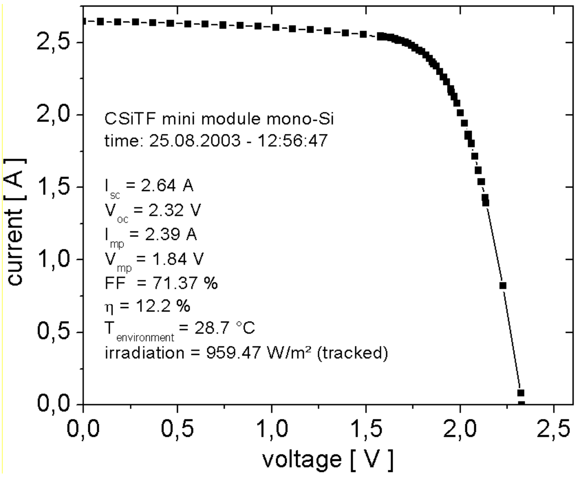

Fig. 5: IV curve of the Cz CSiTF mini module.

The short circuit current of the module, however is approx. 4% higher than that of the worst cell (28.6 mA/cm^2 in module vs. 27.5 mA/cm^2), in spite of a lower irradiation power compared to standard conditions. This effect may be explained by a lower overall reflection since the AR coating of the cells was designed to suit best in encapsulated state. It is remarkable that the I_{sc} value of the module is only slightly lower than the corresponding value of the high-efficiency cells of process A.

3.2.2 Module from multicrystalline CSiTF solar cells

On an aperture area of 576 cm^2, the efficiency of the module made from mc-Si CSiTF cells was measured to be 10.2% at standard conditions. A full set of module parameters can be extracted from figure 6, figure 7 shows a photograph of the module. We were successful to maintain the cell parameters of the solar cells when interconnecting them better than in case of the mono-Si CSiTF cells: the performance drop after interconnection and lamination was about 5%, compared to about 11% in case of the mono-Si module, although the thickness of the anti reflection coating was not optimized for encapsulation. The reason is probably the lower wafer thickness of the mc-Si substrates and with that the more uncritical contact tab soldering.

From the experiences gained in interconnection and encapsulating of epitaxial wafer equivalent solar cells, we do not see any problems in scaling-up. Thus we conclude that also for the module part, solar cells made from epitaxial wafer equivalents are indeed fully compatible to a standard wafer solar cell.

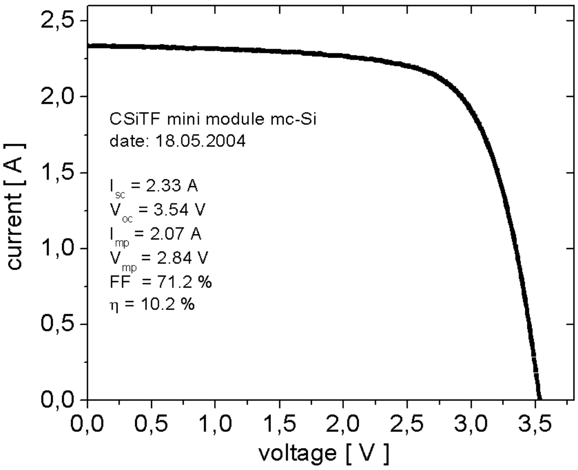

Fig. 6: IV curve and module parameters of the mc-Si CSiTF mini module.

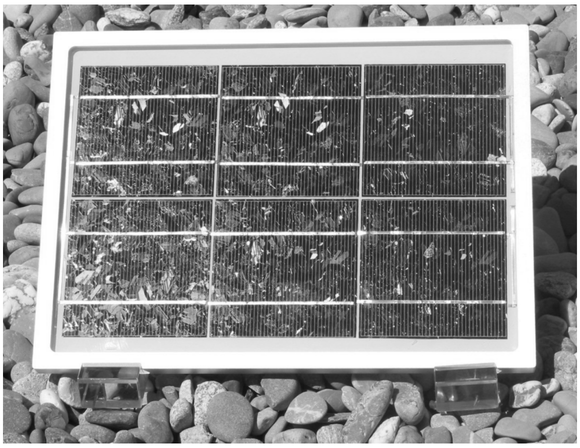

Fig. 7: Picture of the module made from mc-Si CSiTF solar cells.

4 CONCLUSIONS

We have manufactured large-area solar cells from epitaxial silicon layers on mono-Si and multi-crystalline silicon substrates (epitaxial wafer equivalents). A variety of processes ranging from high-efficiency process to production-type process were applied to the different wafer equivalents, in order to test their performance in processes with different complexity. It could be shown in all processes, that epitaxial wafer equivalents of the same thickness as standard silicon wafers are fully compatible to the usual processes. The best cell result of 15.2% could be achieved with a high-efficiency process on a cell area of 143 cm^2. All cells however are limited in short circuit current by the loss of long-wavelength photons due to the short optical path in the active layer.

For module manufacturing, also standard processes could be applied to the thin-film solar cells. Two mini modules were made, using either mono-Si or multi-crystalline silicon wafer equivalent solar cells. Their efficiencies of 12.2% and 10.2%, respectively, proves, that module efficiencies significantly higher than 10% are possible with CSiTF solar cells made in high-temperature approach. Further potential to improve the efficiency clearly lies in better light trapping to increase I_{sc}, which should be one main focus of further work, in addition to application of real low-cost substrates and epitaxy.

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