

## INTEGRATED INTERCONNECTION OF CRYSTALLINE SILICON THIN FILM SOLAR CELLS

Regina Pavlović, Stefan Janz, Stefan Reber  
Fraunhofer Institute for Solar Energy Systems  
Heidenhofstraße 2, D-79102 Freiburg, Germany  
Phone: +49 761 4588 5591, fax: +49 761 4588 9250  
E-mail: regina.pavlovic@ise.fraunhofer.de

**ABSTRACT:** A concept for integrated interconnected crystalline silicon thin film solar cells is presented. Following the classical thin film approach the crystalline silicon thin film is divided into individual cell stripes and interconnected monolithically, directly on the substrate. Taking advantage of the crystalline quality of the material, the interconnection is realized using screen printing pastes. In this paper we focus our experimental investigations on the separation of cell stripes and the interconnection via screen printing. The cell separation is either done by oxide masking and KOH etching or by laser ablation and a subsequent etch step. For the interconnection not only metallization pastes are required, but also an isolating material to protect the edge of the cell against shunting. Different isolating screen printing pastes were tested for their isolation properties against metallization pastes. In further experiments the influence of different firing parameters was investigated.

The cell stripe width strongly affects the series resistance of the module, since it is a single side contacted concept where only the back surface field (BSF) is responsible for the electrical conductivity on the rear. Therefore the series resistance is estimated in dependence on the cell stripe width.

**Keywords:** Crystalline Silicon, Thin Film, Monolithic Interconnection, Screen Printing, Isolation

### 1 INTRODUCTION

The crystalline silicon thin film solar cell technology attempts to combine the advantages of both thin film and wafer technologies to reduce the cost of solar cell production. At Fraunhofer ISE tools for large-area zone melting recrystallization [1] and epitaxial silicon deposition [2] are under development. These tools enable the manufacture of thin crystalline silicon films in module size on low-cost substrates.

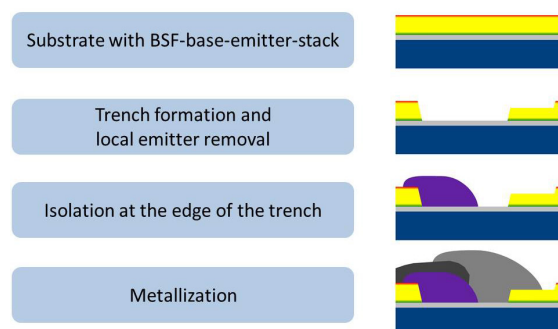
In order to use the potential of large-area crystalline silicon thin films an efficient module interconnection concept is required. Following the classical thin film approach cell stripes are separated and interconnected directly on the substrate. This leads to a soldering-free module interconnection, increases the active module area and simplifies the production process of the module.

Even though a thin film approach is chosen it is combined with wafer technologies to gain advantage of the usage of crystalline silicon. For one, crystalline silicon has a sufficient conductivity, so there is no need for a transparent conductive oxide (TCO) layer and, using fingers, it should be possible to choose a larger cell stripe width and hereby further increase the active cell area.

This work focusses on industrially feasible processing steps such as laser ablation processes for cell separation and screen printing for metallization. Additionally an estimation of the impact of the cell stripe width on the active cell area as well as the series resistance is given.

### 2 INTEGRATED INTERCONNECTION CONCEPT

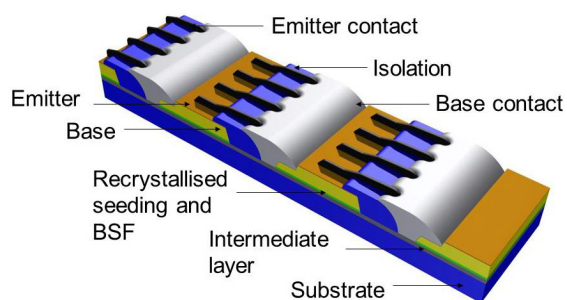
The process (see Figure 1) is started with a silicon layer stack consisting of back surface field (BSF), absorber and emitter on an intermediate layer on a substrate. Substrate and intermediate layer have to be high temperature stable as high temperature processes are used for the silicon layer preparation.



**Figure 1:** Processing sequence for the integrated interconnected thin film module.

There are different ways to generate this silicon layer stack. It can be a recrystallized and epitaxially thickened layer on an insulating substrate (e.g. ceramics) with intermediate layer [3]. The recrystallization is usually carried out by zone-melting of a seeding layer, deposited on the intermediate layer by atmospheric pressure chemical vapor deposition (APCVD) [4]. The epitaxial layer is also deposited in an APCVD reactor. The silicon layer stack can also be bonded on an insulating substrate or insulating intermediate layer. The cell concept would remain the same, only few processing steps would have to be adjusted. In this case also a low-temperature process could be applied to enable the use of a transparent substrate.

First the cells need to be separated into stripes and the emitter has to be locally removed. To prevent shunting, an isolation material has to be applied at the edge of the trench. As this material has to isolate against the emitter metallization, it has to be optimized along with the metallization step. The last step is the metallization which includes the interconnection. A module detail can be seen in Figure 2.



**Figure 2:** Detail of module with integrated interconnection. (Not to scale.)

Texturization and application of a passivation layer are not shown in Figure 1, but could be performed at different points depending on the methods used.

Two crucial steps in the process are the trench formation and the isolation of the trench edge. Not completely separated cell stripes or a shunt at the trench edge would cause shorting of the module. In the following paragraphs possible ways of realizing trench formation and edge isolation are discussed.

### 3 TRENCH FORMATION

Two approaches were investigated to form the trench between the individual cells. One was to mask the surface with a structured thermally grown oxide and perform a KOH etch to separate the cells. As an industrially more feasible process, trench formation by laser ablation was studied. To ensure the electrical isolation of the cell stripes and remove residual silicon and laser induced damage in the trench, a subsequent etching step is applied. In this work a short KOH or plasma etch was investigated.

#### 3.1 Trenches by wet chemical etching

To separate the cell stripes by KOH etching (40% aqueous KOH, 80°C), a long (approximately 30 min) etch step is required as the silicon absorber layer is 20 to 30  $\mu\text{m}$  thick. The masking layer has to withstand the long etching time and be structurable. We chose a thermally grown oxide as masking layer and structured it by a photolithography process. This approach led to uniform separating trenches on (100) oriented wafers.

Forming the trenches by KOH etching, the crystal orientation of the silicon layer has to be taken into account [5]. As the KOH etch rate is least on (111) oriented surfaces, the slopes of the trench will be (111) oriented. This leads to uniformly shaped trenches on (100) oriented material. If multicrystalline wafers or recrystallized and epitaxially thickened layers were used the etch rate would vary in the different grains. In [6] the etch rate for 40% KOH at 70°C is given for different crystal orientations and ranges from 0.01  $\mu\text{m}/\text{min}$  for (111) surfaces to 1.29  $\mu\text{m}/\text{min}$  for (110) surfaces. With differing etch rates in various grains the etched trenches would vary severely in width and shape, which would make further processing complicated.

#### 3.2 Trenches by laser processing

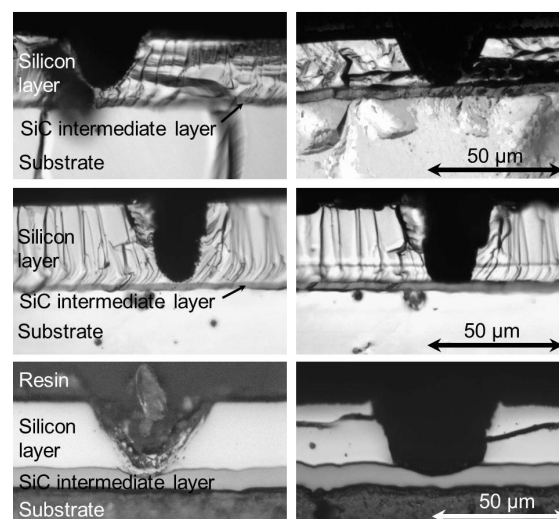
Separating the cell stripes by laser processing does not only involve fewer processing steps but also generates uniformly shaped trenches in multicrystalline

silicon. Trenches formed with different laser parameters in 24  $\mu\text{m}$  to 30  $\mu\text{m}$  thick recrystallized and epitaxially thickened silicon layers can be seen in Figure 3 (left side).

Recrystallized and epitaxially thickened silicon films usually show thickness variations over the sample, caused by orientation dependent growth rates. To account for these irregularities and to remove residual silicon and laser induced damage a subsequent etching step has to be applied.

In Figure 3 optical microscopy images of identical laser trenches before and after a 3 min KOH etch (23% aqueous KOH, 80°C) and before and after a 5 min plasma etch (RF-plasma with  $\text{SF}_6$ ) are presented.

The subsequent etching could also be a texturization in order to combine two different process steps in one. In Figure 3 (bottom) optical microscope images of trenches formed by the same laser process before and after texturization are displayed. In this case we used a plasma texturing process which removes 3  $\mu\text{m}$  of silicon during the process at an etch rate of approximately 0,2  $\mu\text{m}/\text{min}$ .



**Figure 3:** Optical microscope image of different isolating trenches formed by laser ablation. Left side: after laser process. Right side: after a subsequent KOH etch (top), plasma etch (middle) or plasma texturization (bottom).

#### 3.3 Results of trench formation

Separation by oxide masking and KOH etching led to uniformly shaped trenches on (100) oriented samples. The process is not feasible for recrystallized layers, because of the strongly orientation dependant etch rate.

In contrast the trench formation by laser processing is not dependent on crystal orientation. Using KOH for the subsequent etch is not as critical as for full KOH etching since the amount of silicon that has to be etched is much smaller in this case ( $< 5 \mu\text{m}$ ). In the plasma etching steps no influence of grain orientation could be observed. They would therefore be well suited for recrystallized material. Due to the subsequent etching step a broad range of laser parameters can be used to generate the trenches, as can be seen in Figure 3.

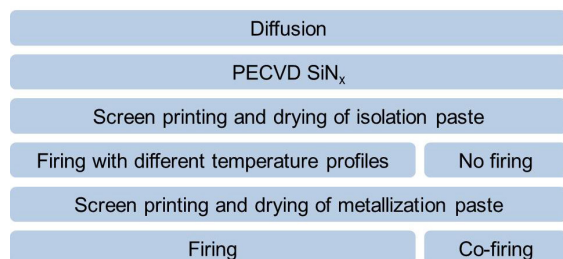
#### 4 ISOLATION MATERIAL

The isolation material depends decisively on the metallization method and materials. If e.g. the contacts are formed by evaporation, a silicon nitride layer should be sufficient as isolation. As we decided to realize the metallization by screen printing, the isolation material has to isolate against silver screen printing pastes. Following our approach the isolation material should also be applied by screen printing. We could find three different screen printing pastes that seemed to be suitable as isolation.

Test structures were made in order to determine the isolating properties of the materials against different silver screen printing pastes and the optimum firing parameters.

##### 4.1 Preparation of samples

For the test structures on 125x125 mm<sup>2</sup> pseudo-square wafers, a 75 Ω/□ emitter was formed by phosphorus diffusion and a SiN<sub>x</sub> layer was deposited by plasma enhanced chemical vapor deposition (PECVD). Four 5x5 cm<sup>2</sup> areas per wafer were defined and the isolation paste was applied. Two of them were fully covered, one was covered partially and one was left uncovered as reference area. In the first experiment, the isolation layers were all fired according to manufacturer's data, about 30 min with peak temperatures of 580 to 850°C. Afterwards the metallization was applied and fired (see Figure 4). Some adhesion problems arose (see section 4.2) and the firing processes for the isolation layers take relatively long. Therefore, in a second experiment, different firing profiles were tested, for the isolation layers, to improve the adhesion. Also short firing profiles, similar to metallization firing, and co-firing with the metallization were tried to shorten processing times.



**Figure 4:** Processing sequence for test samples to determine isolating properties of different isolation pastes and to optimize their firing parameters.

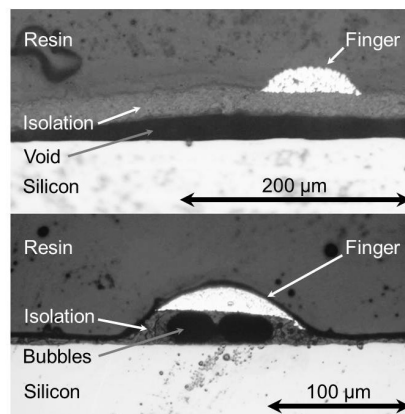
The samples were characterized by transmission line model (TLM) measurements to check, if the silver pastes did form a contact through the isolation and, in the reference areas without isolation, through the subjacent SiN<sub>x</sub> passivation layer.

##### 4.2 Isolation properties

In a first experiment three isolating screen printing pastes were investigated in conjunction with three silver screen printing pastes containing different amounts of glass frit. All isolation layers were fired according to manufacturer's data.

Two isolation pastes isolated against all three silver screen printing pastes. The silver paste had adhesion

problems on isolation paste 2. In cross sections the reason could be found to be in small bubbles within the isolation under the contact fingers (see Figure 5, bottom). With paste 1 adhesion problems of the paste on the wafer occurred (see Figure 5, top). The formation of bubbles in the isolation layer suggests that the adhesion problems might be solved by varying the firing profiles.



**Figure 5:** Optical microscope image of cross section of test sample with isolation layer and metallization. Paste 1 (top) detaches from the wafer at some spots while bubbles are formed in paste 2 (bottom) causing the metal finger to lift off.

The isolation paste 3, that was fired at the lowest temperature, did not form a reliable isolation layer against two of the silver pastes and was not analyzed further. In areas without isolation the silver paste with the highest glass frit content formed the best contact and was used in further experiments.

##### 4.3 Firing profile optimization

To improve adhesion properties and try shortening the process, a firing profile optimization was conducted.

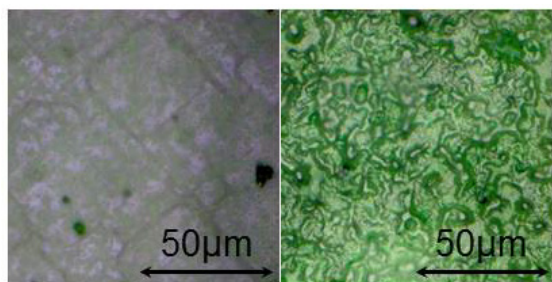
The two isolation pastes that showed good isolation properties were fired with different firing profiles. These included long firing profiles (about 30 min) at different peak temperatures (above 600°C) and short firing profiles similar to a metallization firing profile with different peak temperatures, also one group of samples was not fired before applying the metallization.

The isolation properties of both pastes were not affected by the variation of firing profiles. Even on the co-fired samples the isolation layers could isolate against the silver paste.

Firing isolation paste 1 with a long firing profile at too high temperatures caused severe tension that broke the wafer. However, after any other firing profile, no change in the paste was visible. Short firing profiles above the limiting temperature of paste 1 seemed to have a negative effect on the adhesion of the paste. Although the adhesion problems with paste 1 could not be fully avoided, long firing profiles at lower temperatures led to better adhesion of the isolation layer on the silicon nitride. Similar results could be obtained by co-firing the isolation with the metallization.

Paste 2 shows a clear difference in color before and after firing. Choosing a long firing profile above the limiting temperature of paste 2 caused the paste to blister (see Figure 6). However, the blistering had a positive impact: The isolation properties were not affected and the

adhesion of the metallization was very good, since no bubble formation beneath the contacts occurred. A short firing profile and co-firing with the metallization led to better adhesion than a long firing profile at temperatures below the limiting temperature. However, these isolation layers could not perform as well as the blistering layer. An overview of the influence of firing parameters on the adhesion of paste 1 on the wafer and the metallization on isolating paste 2 is presented in Table 1.



**Figure 6:** Optical microscopy images of paste 2 after a long firing step at different temperatures: Lower temperature (left) and higher temperature (right).

**Table 1:** Adhesion quality depending on firing parameters. In case of paste 1 the adhesion of the isolation layer to the wafer is considered, in case of paste 2, the adhesion of the metallization to the isolation layer.

Firing parameters	No firing	Short firing	Long firing profile		
			Increasing Temperature →		
Paste 1					Wafer breakage
Paste 2					Blistering Not performed

Good adhesion	Medium adhesion	Bad adhesion
---------------	-----------------	--------------

#### 4.4 Results of isolation material

Summing up, we could find two different screen printing pastes with excellent isolating properties. For paste 2 the firing parameters were optimized and the adhesion problems solved. The structure of our test samples is much more challenging concerning adhesion than our final application, since in the interconnection concept the isolation is only applied at the trench edge and the silver fingers run across it perpendicularly. Therefore both pastes should be suitable for this cell concept.

### 5 OPTIMUM CELL WIDTH

In this concept the rear side of the cell is only contacted on one side by the base contact. Without any contacts across the back of the cell, the BSF is responsible for the electrical conductivity at the rear. Therefore the cell stripe width has considerable influence on the series resistance. On one hand the series resistance of the module increases with increasing cell stripe width, on the other hand the active module area decreases with increasing cell stripe width.

It should also be noted that by varying the cell stripe width and number of cells in a module, current and voltage of the module can be adjusted.

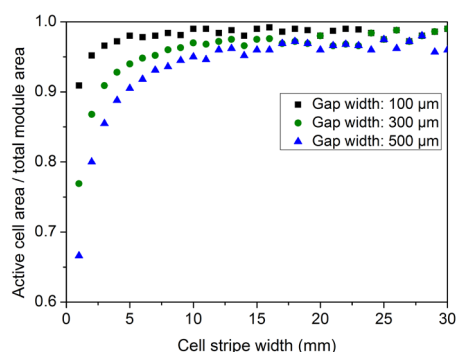
In the following an estimation of the dependency of the active module area fraction and the series resistance on the cell stripe width is given.

#### 5.1 Active cell area

The active cell area in this concept equals the module area reduced by the gap between the individual cell stripes which is needed to form the interconnection.

The fraction of the active module area is estimated for a module width of 1 m. As the cell stripes are arrayed lengthwise, the active module area fraction is independent of the module length. The module frame was not taken into account.

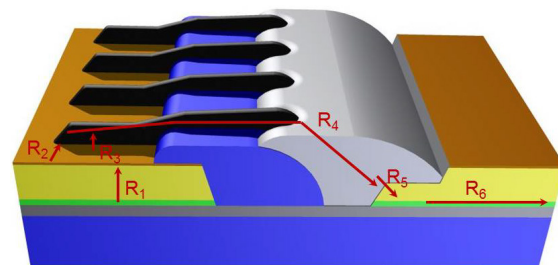
In Figure 7 the fraction of the active cell area is plotted against the cell stripe width for different gap widths. It can be seen, that the influence of the gap width decreases considerably with increasing cell stripe sizes.



**Figure 7:** Fraction of active module area depending on the cell stripe width and the gap needed for interconnection between the cells.

#### 5.2 Series resistance contributions

The series resistance was estimated accumulating the respective resistance contributions of the cell as described in [7]. In this cell structure the following could be identified (see Figure 8): The resistance of BSF and base ( $R_1$ ), the resistance in the emitter ( $R_2$ ), the contact resistance of the emitter contact ( $R_3$ ), the resistance in the metallization ( $R_4$ ), the contact resistance of the base contact ( $R_5$ ) and the resistance of the BSF along the width of the cell ( $R_6$ ).

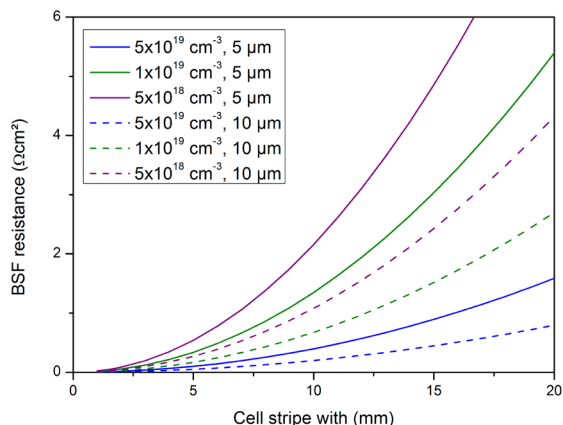


**Figure 8:** Schematic of the interconnection (not to scale) with the respective resistance contributions.

A couple of assumptions were made to estimate the series resistance: (i) A 30  $\mu\text{m}$  thick absorber with (ii) a conductivity of 0.5  $\Omega\text{cm}$  was used. (iii) The finger spacing was set to 1.5 mm and (iv) screen printing contacts were assumed, with (v) a local BSF forming beneath the aluminum base contact [8]. (vi) The contact areas of base and emitter contact were set to be equal.

(vii) The contact resistance between the two different metal pastes was not taken into account.

As mentioned before, the series resistance is influenced strongly by the conductivity of the BSF. Varying its thickness and doping concentration has a significant impact on the series resistance contribution of the BSF ( $R_6$ ). In Figure 9 the series resistance contribution of the BSF is shown for different doping concentrations and thicknesses. In the following sections we calculated with a 5  $\mu\text{m}$  thick BSF with a doping concentration of  $5 \times 10^{19} \text{ cm}^{-3}$ , which is the current boron doping limit in our lab type APCVD reactors.



**Figure 9:** BSF resistance for different doping concentrations and thicknesses dependent on the cell stripe width.

The cell stripe width was varied from 2 to 20 mm. As the finger distance was set to 1.5 mm, a cell stripe width equal or smaller than 1.5 mm would not require fingers perpendicular to the base contact at all. In this case a different metallization geometry would be used.

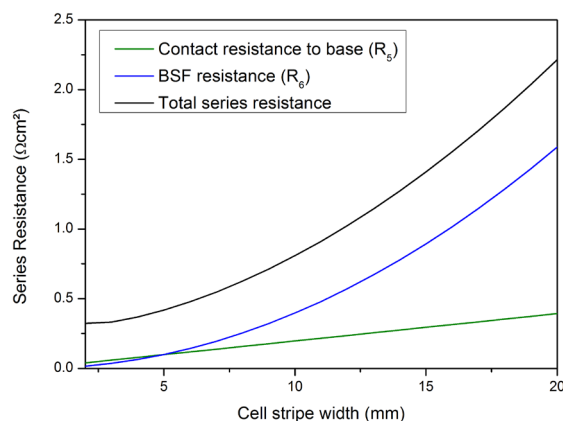
Three partial resistances do not contribute to the total series resistance significantly: The resistance of BSF and base ( $R_1$ ), the contact resistance between metallization and emitter ( $R_3$ ) and the resistance in the metallization itself ( $R_4$ ). The resistance in the emitter ( $R_2$ ) does not depend connotatively on the cell stripe width as it depends mostly on the finger spacing. These will not be examined further.

### 5.3 Series resistance dependency on cell stripe width

The graph in Figure 10 displays the total series resistance and the two major contributors dependent on the cell stripe width.

The resistance of the BSF certainly has the main share of the total series resistance. It is therefore likely that the BSF conductivity is the most limiting factor concerning wider cell stripes. Adjusting thickness and doping of the BSF, the resistance can be varied accordingly (see Figure 9).

The contact resistance between Al-finger and base is increasing linearly with wider cell stripes, because the contact area of the base contact remains the same. As more current is generated in a larger cell, it might be necessary to use a wider base contact. This way the contribution of the base contact resistance to the total series resistance can be reduced.

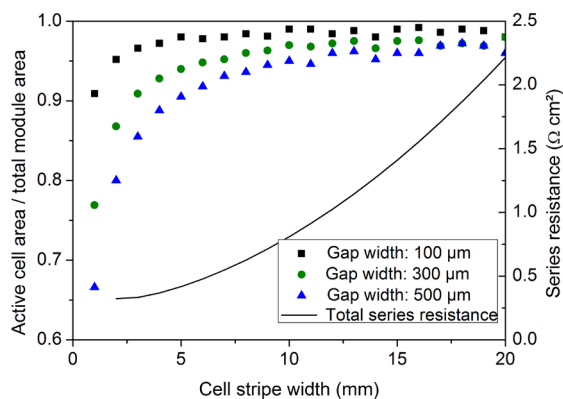


**Figure 10:** Series resistance and the two major contributing resistances in dependence of cell stripe width.

### 5.4 Series resistance and active module area

For small cell stripes the width of the interconnection gap plays an important role. Wide cell stripes, on the other hand, lead to a strong increase in series resistance, but a better active cell area fraction (see Figure 11).

To achieve an active module area fraction above 85% even for a gap width of 500  $\mu\text{m}$ , the cell stripe width has to be at least 3 mm. Furthermore, the cell stripe width should not exceed 10 mm to ensure a series resistance below  $1 \Omega\text{cm}^2$ . Especially in the range from 3 to 10 mm cell stripe width, the gap width influences the active module area fraction strongly. Process optimization to reduce the gap width is therefore profitable.



**Figure 11:** Series resistance and active cell area dependent on the cell stripe width.

## 6 SUMMARY AND OUTLOOK

An interconnection concept for crystalline silicon thin film solar cells on insulating substrates was presented.

The separation of cell stripes was implemented by two different methods. For monocrystalline silicon the KOH etching is a reliable method. To simplify the process it could be possible to use a PECVD oxide or nitride instead of the thermally grown oxide, though pinholes should be avoided. Thus the number of high temperature steps could be reduced.

The laser ablation process with subsequent etch step is an effective way to realize cell separation, which is feasible for mono- and multicrystalline silicon layers. In

this case the possibility to combine the subsequent etching with a texturization step is particularly appealing.

Independent of the trench formation itself, the electrical properties of the trench have to be studied to determine the amount of damage induced by each method.

The investigation of different isolating screen printing pastes showed excellent results concerning the isolation properties of two of the pastes. Occurring adhesion problems could be completely solved for one of the pastes. In the next step the minimum firing time at which the blistering of the paste occurs will be determined, as a short firing step is preferred. As the test structure is more challenging concerning adhesion issues than our final cell structure, possibly both pastes could be used. Also the screen printing of the isolation layers at the trench edge has to be investigated.

Estimating the series resistance of the cell concept, the BSF sheet resistance could be identified as the main contributor. Thickness and doping of the BSF should be adjusted to the cell stripe width. The series resistance was compared to the active cell area in dependence of the cell stripe width. Cell stripes widths in the range of 3 to 10 mm should be used to keep the series resistance at an acceptable level (below  $1 \Omega\text{cm}^2$ ) as well as the active module area (above 85%). In this range the width of the interconnection gap plays an important role and work should be done to minimize the interconnection gap. Damaged material at the trench edges could also affect the cell performance and shift the optimal cell stripe width to wider cell stripes. To identify the optimum cell stripe width, experiments have to be done to determine the actual series resistance, gap width and damage due to trench formation.

## 7 ACKNOWLEDGEMENTS

The authors would like to thank DuPont and Heraeus for providing the investigated isolating materials and all colleagues at Fraunhofer ISE who contributed to this paper in general. Parts of this work have been supported by the European project "R2M-Si" under the contract number 256762.

## 8 REFERENCES

- [1] S. Reber, A. Eyer and F. Haas, "High-throughput zone-melting recrystallization for crystalline silicon thin-film solar cells," *Journal of Crystal Growth* 287, p. 391–396, 2006.
- [2] S. Reber, M. Arnold, D. Pocza and N. Schillinger, "ConCVD and ProConCVD: Development of high-throughput CVD tools on the way to low-cost silicon epitaxy," in *Proceedings of the 24th European Photovoltaic Solar Energy Conference*, Hamburg, 2009.
- [3] K. Schillinger, S. Janz and S. Reber, "Atmospheric Pressure Chemical Vapour Deposition of 3C-SiC for Silicon Thin-Film Solar Cells on Various Substrates," *Journal of Nanoscience and Nanotechnology*, Vol. 11, p. 8108–8113, 2011.
- [4] T. Kieliba, J. Pohl, A. Eyer and C. Schmiga, "Optimization of c-Si films formed by zone-melting recrystallization for thin-film solar cells," in *WCPEC3-Conference*, Osaka, 2003.
- [5] H. Seidel, L. Csepregi, A. Heuberger and H.

Baumgärtel, "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions," *J. Electrochem. Soc.*, Vol. 137, pp. 3612-3632, 1990.

- [6] K. Sato, M. Shikida, Y. Matsushima, T. Yamashiro, K. Asaumi, Y. Iriye und M. Yamamoto, „Characterization of orientation-dependent etching properties of single-crystal silicon: effects of KOH concentration," *Sensors and Actuators A Vol.64*, pp. 87-93, 1998.
- [7] A. Goetzberger, B. Voß and J. Knoblich, *Sonnenergie: Photovoltaik*, Stuttgart: B. G. Teubner, 1997.
- [8] J. Krause, R. Woehl and D. Biro, "Analysis of local Al-p<sup>+</sup>-layers for solar cells processed by small screen-printed structures," in *Proceedings of the 25th European Photovoltaic Solar Energy Conference*, Valencia, 2010.