

Design of a 12-bit cyclic RSD ADC Sensor Interface IC using the Intelligent Analog IP Library

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Abstract

Within this paper we present an Intelligent Analog IP design flow and its successful application on an industrial-level mixed-signal ASIC design. This novel design flow is based on a library of flexible (configurable), robust (Design for reliability awareness) and technology-independent Analog IPs, available from primitive device level up to complex circuit blocks. Its application leads to a significant increase in efficiency of the overall design process due to reduced design and layout cost, speed-up or even avoidance of redesign cycles and very fast technology porting. For the design of a multi-physical SMART sensor interface with a low-power 12-bit RSD ADC we already saved 43 % of layout time using the Intelligent Analog IP design flow. In addition, system-level and schematic design as well as post-layout verification was more efficient compared to conventional design flows.

1 Introduction

Analog parts of mixed-signal circuits like interfaces for sensor signal processing still cause a huge amount of total design effort. For typical, digital dominated mixed-signal ICs with an area share of 10 to 30 % for the analog parts, this analog design effort may have an amount of up to 80 %.

The well-known reason is the much higher complexity of performance and parameter constraints of analog blocks and the resulting lack of mature automation tools like topology and layout synthesis known from digital IC design. The large amount of manual work leads to a strong dependence of design quality on the individual designer's experience and thus to a higher sensitivity to expensive re-design cycles due to parasitic effects or bad yield with again large effort for circuit sizing or even topology change and layout. The same effort is usually needed for technology migration.

General approaches to address this problem would be:

- Avoid analog circuits. This is partly addressed by using the high computing power of today's digital ICs e.g. for advanced signal processing in wireless applications, but each sensing or wireless application still needs at least amplifiers and data converters for signal conditioning.
- Decrease complexity. In the digital world this is achieved by the (re-)use of standard cells. These pre-characterized IP blocks with known behavior and properties significantly limit the space of possible topologies, sizing and layout variants for the final circuit.
- Handle complexity. This includes all automatizations that support the design and layout engineers with their daily tasks. Examples are fast search algo-

gorithms for appropriate topologies (synthesis) [1], device sizing with optimization of circuit performances and parametric yield [3], automatic placement and routing based on matching and geometrical constraints.

Even though several new approaches for analog design and layout automation were presented during the last decade [1][4][5][6][7][8][9], we still see conventional, handwork-dominated design cycles and layout implementation practiced by the major part of analog design teams. Established EDA design environments like Cadence Virtuoso GXL provide several new features for automatic sizing, placement and routing of analog circuits, but they still show several problems [2] and are mainly intended to just increase productivity of single design steps, not to change them.

Our resume is that a combination of the latter two approaches – *decrease* and *handle* complexity – would be the most promising solution for a faster and more reliable analog circuit design flow. This led to the idea of the Intelligent Analog IP library (Section 2). Complexity is *decreased* and design know-how is retained by IP re-use, which limits the variety of possible topologies to pre-defined, hierarchical, general-purpose analog IP blocks from which a designer or optimization algorithm can choose to create new circuits. The remaining complexity and necessary flexibility is *handled* by the “intelligence” of the IPs and the design flow (Section 3): parameters to adapt performance and layout properties of the IP, common generation of consistent schematic and layout views of the IP, automatic consideration of design rules, matching and reliability constraints during layout generation, parasitic-aware circuit optimization flow.

A further important and often underestimated requirement of successful design flow improvements is usability and

acceptance by the designer community. Main issues are compatibility with established design tools and PDK environments, low initial effort, low maintenance effort, stability and design flow reliability. The Intelligent Analog IP approach addresses these issues by using standard EDA tools like Cadence Virtuoso and MunEDA WiCkeD, scalable use of the Intelligent IPs up to system level complexity, and reproducible design steps due to executable generic circuit descriptions.

2 Intelligent Analog IP Library

The term Analog IP in this context denotes (sub-)circuits which can be used as building blocks to design more complex analog/mixed-signal circuits. Such IP blocks are usually represented by design views like behavioral model, transistor-level schematic, and layout in a design database. One IP block can be composed of several sub-blocks in a hierarchical way. In our case, the IPs are represented by generator programs that can dynamically create the target views in the database. These generators are implemented based on the design environment’s scripting language (SKILL in case of Cadence) and the 1Stone programming interface [10].

Generator Hierarchy Levels	Example IP	Status	Re-use per 10 designs
System	sensor systems	generator not implemented	0 .. 1
High	ADC, DAC	productive use / full demo scheduled for summer 2013	1 .. 3
Mid	special op-amps, VCO, bandgap	demo available / productive use / further IPs in progress	1 .. 10
Low	simple op-amps, current source, comparator	demo available / productive use / further IPs in progress	1 .. 50
Base	current mirror, diff pair, cap array, res array	productive use	> 200
Device	MOS, C, R	productive use	100%

Table 1 Structure of the Intelligent Analog IP library

The Intelligent Analog IP library contains IP generators for usual analog building blocks as well as for system-level blocks. To gain maximum IP re-use, there are separate generators for blocks at each different circuit hierarchy level, and the generators of higher-level blocks use instances of lower-level generators for nearly all sub-elements. Table 1 gives an overview on the structure and current implementation status of the library. It also shows for each hierarchy level the mean number of IP occur-

rences, which can be seen as the maximum possible re-use of the corresponding IP generators.

For the lower hierarchy levels, the high re-use factor leads to higher demands on universality and parametric variability of the generator programs. Especially the independence from a certain technology or PDK has to be ensured by the device- and base-level generators.

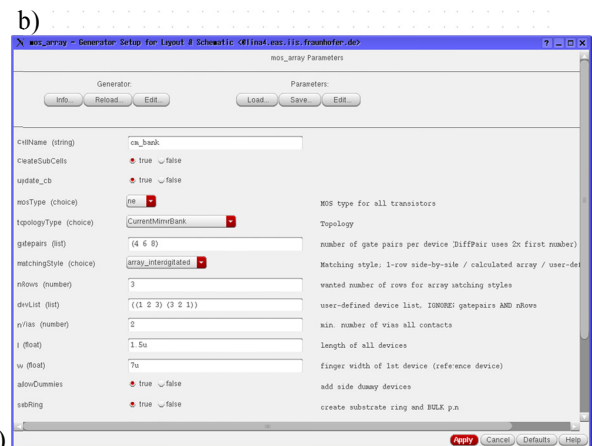
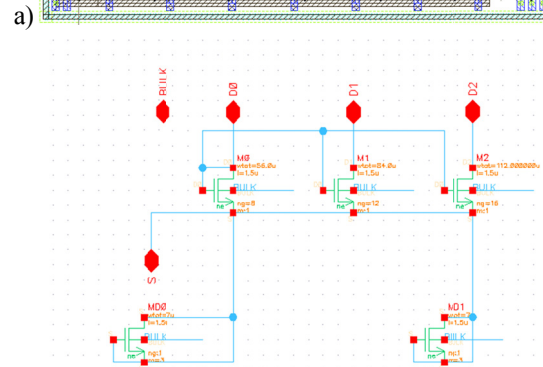
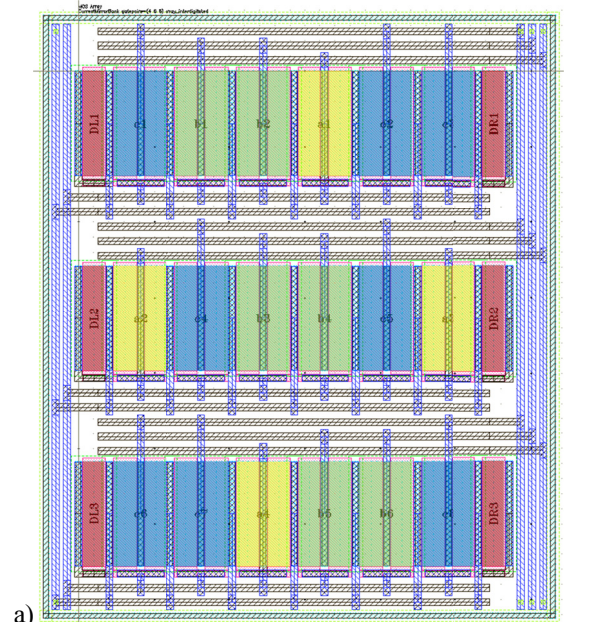


Figure 1 Current mirror bank using common centroid array arrangement with dummies, generated by the base-level generator “mos_array” within Cadence design environment: a) layout view in XFAB 180 nm process, b) schematic view, c) parameter mask

At device level the library provides generators for primitive elements like MOS transistors, capacitances, and resistors. These device generators create a symbol view for instantiation of the element within a schematic, and a layout view. The symbol view is directly taken from the target PDK to ensure that the right device models, provided by the foundry, are used during simulation. The generator automatically selects and parameterizes the corresponding PDK device depending on its own parameter settings. For the layout it depends on the target technology whether the generator also instantiates the device directly from the PDK or generates it dynamically to be independent from PDK-specific restrictions regarding e.g. contact arrangement or callback functions.

An essential goal of the generator approach is to create design-rule-compliant layouts for each parameter setting and at each hierarchy level. This is obtained by the definition of reference coordinates that indicate e.g. the location of pins or layer borders for a generated layout. These coordinates are then used during instantiation in the next hierarchy level to ensure a relative placement of all elements without detailed knowledge about the internal layout structure of the sub-block to be instantiated. This feature is most important for the device-level generators as part of the technology mapping and is provided by the programming interface of the 1Stone environment.

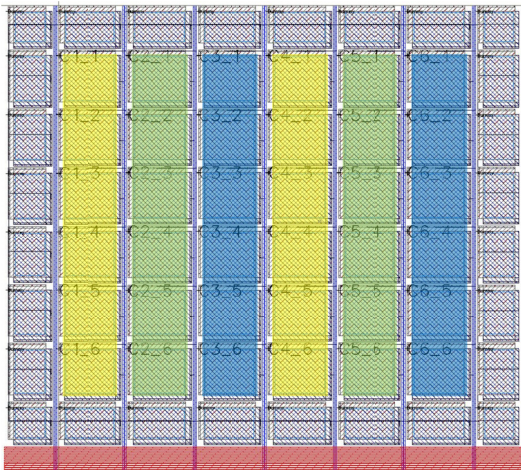


Figure 2 Interdigitated layout of three matched capacitances with dummies, created by the base-level generator “cap_array”

At base level we implemented generators for primitive circuits based on the three types of primitive devices supported by the device-level generators: *mos_array*, *cap_array*, and *res_array*. A generator for bipolar transistor devices is under construction. These array generators provide very basic topologies used in most types of analog circuits like current mirrors or differential pairs. The possible complexity reaches from single devices up to large array structures with interdigitated or common-centroid arrangement of several different devices for high matching or e.g. precise voltage divider circuits. To simplify library usage and maintenance we decided to use these base-level generators as the lowest hierarchy in designs based on our IP library. This allows to change or

even replace the device-level generation code, e.g. for adapting it to new technologies/PDKs, without interfering design steps.

Two examples of base-level generators are given in Figure 1 and Figure 2. They also show the application of further “intelligent” algorithms on layout generation like the calculation of best matching arrangements based on a given array size and numbers of elements per device. The base-level generators additionally allow the user to define the maximum width/height of the final layout which is achieved by an automatic adaption of size and arrangement of the array elements.

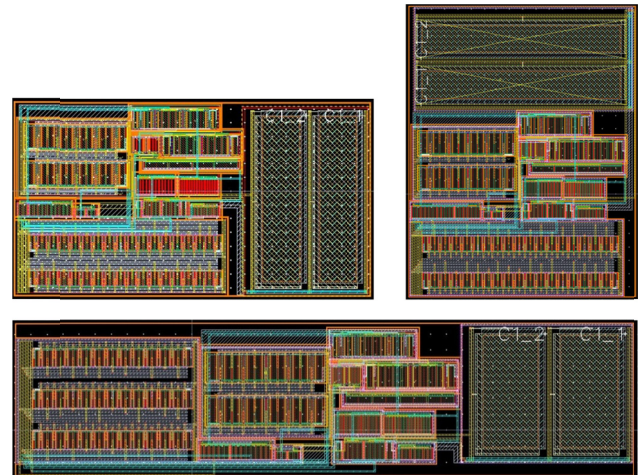


Figure 3 Generated layouts for three different specifications out of one generator for a single-ended op-amp: a) fast variant with compact layout b) low-power variant with vertical layout c) medium-power variant with wide layout

As an example of a mid-level generator, Figure 3 shows three variants of the single-ended op-amp used in the sensor IC presented in Section 4. The variants differ in performance and also layout arrangement. The performance-relevant design parameters were determined by a sensitivity analysis of the circuit topology and provided as generator input parameters. The values of these parameters were then found by the optimization tool WiCkeD for the different target specifications. The changeable layout arrangement is an additional feature that allows the adaption of the op-amp instance to the surrounding layout. In total eight instances of this generator were used in the sensor IC.

Due to the reduced possible re-use factor of the higher hierarchy levels the benefit of such generators will strongly depend on future application of the circuit with changed specification or technology. Thus, we did not implement a top-level generator of the SMART sensor IC yet. At high level, however, data converters like RSD ADCs offer some re-use potential by generating tailored variants for different resolutions, pipelined or cyclic architectures, and stages with different accuracy demands. A generator for a more sophisticated RSD ADC architecture is currently under construction and scheduled as the next milestone to demonstrate the potential of the Intelligent Analog IP library.

3 Intelligent Analog IP Design Flow

A design flow describes a sequence of tasks to be executed to reach the design goal. In the literature circuit design flows are usually divided into bottom-up and top-down approaches. The Intelligent Analog IP library was started with the implementation of schematic and layout generators for lower circuit hierarchies – thus, the focus was on bottom-up design. With more complex IPs and the knowledge of their properties also top-down design at these higher hierarchies is possible due to the implementation of parametric behavioral models within the IP generators.

As motivated in Section 1, the Intelligent Analog IP design flow is a combination of complexity decrease by using pre-defined IPs, and complexity handling. This is the way we identified as most viable towards an applicable analog synthesis.

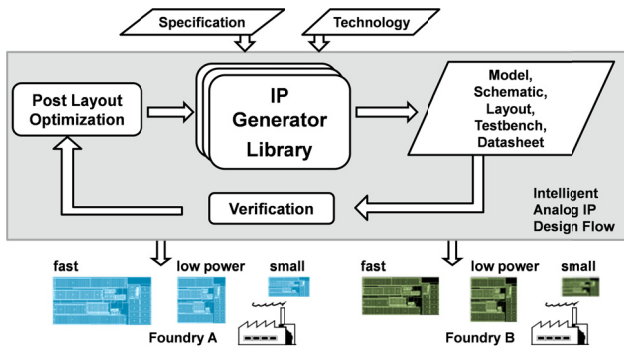


Figure 4 Intelligent Analog IP Design Flow

To keep acceptance of a design team, the IP library approach provides a good scalability in terms of use cases. At a first stage the Intelligent IPs could simply be used like hard IPs with fixed parameterization. The generators allow direct instantiation of the parameterized design views from the design environment’s schematic and also the layout editor. Once generated, they can be used and even further adapted like any other circuit element. This use case has a low initial effort but of course, re-use is limited and re-generation would overwrite manual changes.

At a next stage, single blocks up to a certain hierarchy could be designed by library IPs exclusively. This includes schematic design using symbols from the generated IPs only, circuit sizing by means of the generator parameters, placement and top-level routing of the generated sub-block layout views. Testbenches and simulation states, generated with some IPs like op-amps can be used, and during layout phase the IPs may further be adapted by parameters that influence their layout view only, like array style, substrate contacts or pin placement. An advanced user may even decide to implement a separate generator for the new block to limit variability to the relevant parameters, add some layout flexibility and enable re-use of the block in further designs and technologies. Without that new generator this use case shows the same low initial effort to get started with the Intelligent Analog IPs. It just requires a convention of the team to use it and

improve design re-use. An important advantage regarding design quality is also the inherent parasitic-awareness of the flow due to the immediately available layout. Thus, layout-dependent effects may already be considered during schematic design.

At a further stage, the sizing process is supported by an optimization tool that automates the loop of parameter change, simulation and verification. It optimizes the performance parameters of the circuit with consideration of device sensitivities, operating points, and process parameters (design centering). In a circuit based on the Intelligent IPs, optimization effort is reduced because of the limited solution space. The IPs provide sizing parameters only for performance-sensitive devices and corresponding value constraints that ensure valid generation results. The exchange of parameters, constraints and optimization results between optimization tool and generator program is supported by a semi-automatic, easy-to-use interface which was successfully applied with Cadence Virtuoso and MunEDA WiCkeD. Additional accuracy is gained when parasitic data from the generated layout is considered by the optimizer. This is realized by using an extracted view with relevant design variables for all simulations during optimization. This post-layout optimization flow [14] was successfully tested in the SMART sensor design (Section 4) with a manual setup. Next step is an automated handling of the design parameters in the extracted netlist.

The current implementation of the Intelligent Analog IP design flow allows a fast, semi-automatic bottom-up design, specification change (re-design) and technology migration of analog circuits. It is illustrated in Figure 4.

With the increasing IP library also a fully automated topology selection, based on a given specification, parameterizable behavioral models of the IPs and an optimizer, becomes conceivable and is point of our current research.

4 SMART sensor design using Intelligent Analog IPs

4.1 Design and implementation

A multi-physical SMART sensor interface chip was designed in different variants using Intelligent Analog IP generators up to high-level complexity. The overall chip consists of integrated sensors for temperature and ambient light as well as a sensitive sensor frontend with high ohmic differential input, addressed to biomedical applications. The core of the chip is built by a single-ended single-stage RSD (redundant signed digit) ADC with 16 bit resolution. In Figure 5 the switching mechanism of the switched capacitor RSD ADC core is illustrated.

A novel architecture with an adjustable offset compensation mechanism is implemented: the last $n-x-1$ LSB (least significant bits) are processed with a conventional RSD algorithm [12]. A number of x SSB (slightly significant bits) are able to compensate operational amplifier offset due to additional phases 2 and 3, where x is adjustable via SPI.

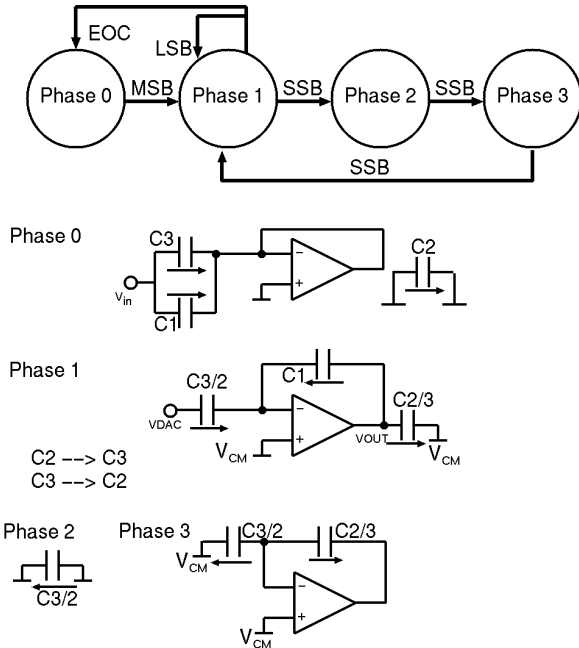


Figure 5 State diagram and switching sequence of the RSD algorithm

Figure 6 shows the physical layout of the high resolution variant of the SMART sensor interface chip with indicated generator usage. In total we implemented 3 different chips using the RSD ADC core IP generator:

- version A: for high-resolution specification,
- version B: for low-power specification,
- version C: for high-speed specification.

In Figure 7 the layouts of the generated RSD ADC core designs with different specifications for version A, B and C are shown.

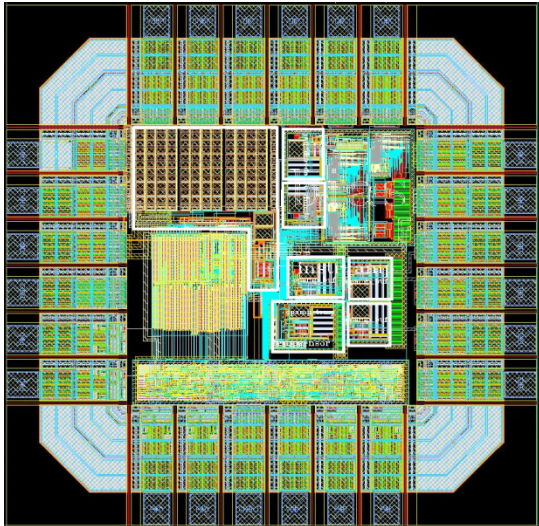


Figure 6 Chip layout of the SMART sensor interface IC with high-resolution RSD ADC. Analog parts, automatically generated by mid- and high-level generators, are indicated with white frames.

Complete designs for different specifications are push-button generated by varying input parameters adjusting operational amplifier gain, settling and power consumption, capacitor and switch size as well as geometric pa-

rameters affecting parasitic coupling and layout shape. The design parameters were determined in a circuit optimization that can be coupled with the generator. All designs were implemented in XFAB 180 nm CMOS technology [13] and were taped-out for fabrication.

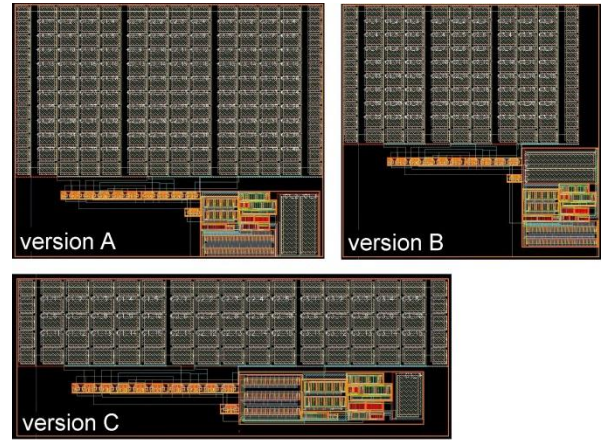


Figure 7 Layouts for three different specifications, generated by the parametric RSD ADC core generator with placement variability: A – high resolution design, B – low power design, C – high speed design

4.2 Postlayout simulation results

In advance to “proof of silicon” we verified the different chip versions using our Intelligent Analog IP generators by postlayout simulation analyses, summarized in Table 2. For comparison reason the commonly used figure of merit $FOM = P/(2^{bit} f_s)$ is given, where P is the power dissipation during conversion, bit is the ADC accuracy and f_s is the sample rate.

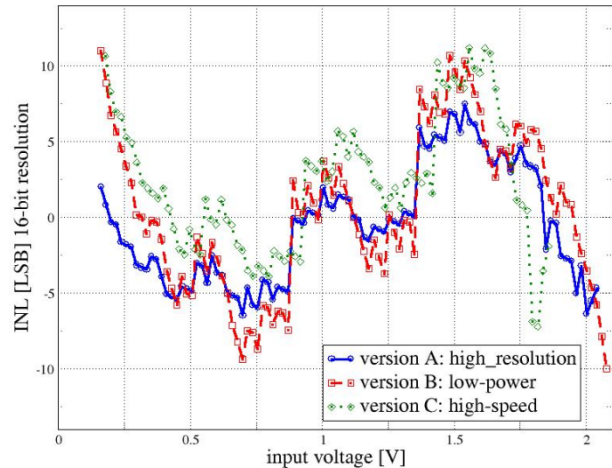


Figure 8 Comparison of ADC accuracy indicator INL with 16 bit resolution for the different chip designs

In Figure 8 the INL (integral nonlinearity) as indicator for ADC accuracy is illustrated for all different versions. We could manage the trade-off between accuracy, speed and power consumption by applying one and the same high-level Analog IP generator for the RSD ADC core. It push-button generated a high-accuracy design with 13.5 bit accuracy (12 bit with offset compensation), a low-power

design with 73 μW power consumption and a significant faster design with 62.5 kS/sec sampling rate.

version	A	B	C
resolution [bit]	16	16	16
accuracy [bit] no offset-compensation	13.5	13.0	10.5
accuracy [bit] 4 SSB offset-compensation	12	11.9	10.0
sampling rate [kS/sec]	12.5	12.5	62.5
power consumption [μW]	248	73	511
input voltage range [V]	2.0	2.0	1.8
FOM [pJ/bit-Conversion]	1.7	0.7	5.6
active chip area [mm^2]	0.4	0.4	0.4

Table 2 Postlayout performance of three different SMART sensor interface chip versions A, B, and C

4.3 Concrete design benefits by using Intelligent Analog IP generators

The postlayout results above clearly show the capability of our parametric Analog IP generators to generate complete designs for a wide specification range within seconds. Beside the enormous reduction of layout cost of 43 % for three chip versions with different specification requirements (see Table 3), we gained a significant efficiency during system-level design and postlayout verification phase. Schematics and layouts were implemented for all three different generator usage levels listed in Table 3. Variants 2 and 3 were taped out for fabrication very recently.

layout method	1	2	3
generator implementation	0	0	5
RSD ADC core layouts A - C	15	11	1
Layout remaining analog parts	20	16	12
Top-level layout	5	5	5
Total effort	40	32	23
Layout cost reduction [%]	0	20	43

Table 3 Comparison of layout cost [in man-day] for three chip designs version A-C for: 1 – conventional hand-made layout, 2 – using base-level generators only, 3 – using up to high-level generators for RSD ADC core

The automated generation of schematics and layouts within a variable design parameter range did speed up system-level and postlayout simulation and analysis. Since we have the layout available immediately after automated IP generation, postlayout optimization [14] within our design flow avoids inefficient over-margin design caused by the discrepancy between pre- and postlayout performances. Furthermore, the reproducibility of design data for all design parameter variations increases design safety and reduces or even avoids redesigns. Since the Intelligent Analog IP generators are technology-independent, we expect a further significant speed-up of technology migration for the presented multi-physical SMART sensor interface chip.

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5 Resume and Outlook

In this paper the successful application of the Intelligent Analog IP library and the corresponding design flow on the design of a multi-physical SMART sensor interface chip is presented. We gained significant efficiency improvements in all design steps from system-level design down to layout generation and verification.

This demonstrates the great potential of our approach to reduce the immense analog design costs and time effort that have to be spent by mixed-signal design companies. This potential may be used to improve flexibility of design services, to implement customer-specific IP generators for external use or even to let customers implement own special IP generators on top of a base library. Our current activities follow short-term and long-term goals. A permanent short-term goal is the maintenance and extension of the Intelligent Analog IP generator library. This also includes support for further PDKs and IP design views like datasheets and especially behavioral and system models. Long-term goals include further flow automation e.g. to consider reliability issues (electromigration, device aging, self-heating, safe operating areas [11]) during layout generation, parasitic-aware circuit optimization, and topology synthesis.

6 References

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