Modeling and Design of a Linear-Assisted Zeta Conveter

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Keywords

«Converter circuit», «Modeling», «Switched-mode power supply», «Emerging topology»

Abstract

Linear-assisted switching (PWM) converters have advantages over single switching topologies, mainly because of the reduction or elimination of bulky output capacitors and ultra-fast dynamical response. In this paper, a linear-assisted zeta converter is presented. The linear regulator circuit is composed by three bipolar transistors and an operational amplifier, which drives the transistor based on the error between the output voltage and its reference. The modeling of the whole circuit is presented, as well as a design example. The modeling of the zeta converter is similar to the conventional topology modeling, except the fact that the linear regulator current is considered as an extra state that substitutes the state regarding the output capacitor voltage. The zeta converter can be designed independently of the linear regulator circuit and simulations are used to validate the static operation of the overall topology. Experimental results confirm in practice the ripple compensation of the main zeta converter, where extra current is provided by the main converter, in order to drive the linear regulator that is responsible for the ripple compensation.

Introduction

Switching regulators, usually pulse-width modulated converters (PWM converters), are widely used in DC-DC converters or AC-DC converters in which a ripple-free DC voltage or a ripple-free DC current is generated at the output. The efficiency of such switching regulator is usually very high, since an adiabatic switching takes place via energy storage. However, it is disadvantageous that such converters require smoothing capacitances at the input and output in order to largely suppress the ripple. Such smoothing capacitors are bulky, and usually life-limiting, in many cases also unsuitable for temperatures above 100 °C.

In order to avoid smoothing capacitors at the output of a switching regulator (PWM converter), a linear regulator can be used instead. The linear regulator supplies the output via an adjustable resistor (controled transistor) in such a way that the output voltage always remains constant [1], [2]. At the same time, this controller would be very fast (bandwidths up to 1 GHz are known) eliminating the disadvantage of limited dynamics. On the other hand, a linear regulator has the disadvantage that the input voltage must always be greater than the output voltage and has a very poor efficiency, which can

be easily below 50% with larger voltage differences between input and output voltage. Therefore very high thermal losses are dissipated in form of heat.

The goal is thus, to take advantage of the switching regulator and the linear regulator at the same time and to avoid their disadvantages in each case. The switching regulators provides steady-state current to the load, while the linear regulator provides higher-frequency transient compensation [3]. Because the linear regulator's transient response compensates the limited transient response of the switching regulator, output capacitance that is commonly required by conventional switching regulators is not needed [4].

Most topologies found in literature regarding linear assisted switching power converters are based on constant voltage outputs. The state-of-the-art is the buck converter with linear regulators in parallel presented in [5],[6] and [7]. The buck converts the input voltage to the output voltage and supplies power to the load, while a linear regulator supplies current from the input to the output and another linear regulator sinks current from the output of the buck converter to the ground. These solutions may present a high efficiency topology with ripple-free output voltage, however it requires the input voltage to be always larger than the output voltage. As a promising solution the PWM Zeta converter may be employed as a step up/down converter of non- inverting polarity type and it can be designed to achieve low-ripple output current [8].

Considered by many designers as an "exotic" topology, the zeta converter (also known as the inverted SEPIC) offers certain advantages over the classical SEPIC. This topology has the same buck-boost functionality as the SEPIC, but the output current is continuous, providing a clean, low-ripple output voltage [9]. This low-noise output converter can be used to power certain types of loads, such as LEDs [10], which are sensitive to the voltage ripple. The zeta converter offers a DC isolation between the input and output, which is attractive when there is risk of short-circuit in the output. This topology can also offer high efficiency, especially if the synchronous switching scheme is used. The synchronous rectification can be easily implemented here, because this topology uses a low-side rectifier.

A complete steady-state characterization for coupled inductor PWM zeta converter with linear assistance is provided in this paper. The zeta converter is first modeled as a conventional topology, except by the fact that the linear regulator current is considered as an extra state that substitutes the state regarding the output capacitor voltage. Then, the linear regulators are modeled as three different paths, which the operation depend on a function of the input and output voltage. The small signal modeling of each linear regulator path is presented, allowing one to previously know the required supply voltage of the operation amplifier. A design example is presented and the components of the zeta converter are selected from the shelf on available markets. In this paper, the dynamical and control considerations are not taken into account, so the static operation is validated through simulations. Finally, a proof of concept is presented and experimental results are obtained to confirm the ripple compensation of the linear regulator in parallel with the zeta converter without output electrolytic capacitor.

Modeling of the linear-assisted zeta converter

The topology is shown on Fig. 1. This linear-assisted converter consists of a PWM zeta converter and three linear regulators (LRs) connected in parallel. The zeta converter supplies the load R_L from an input voltage V_{in} and converts it either up or down to the desired output voltage V_{out}. The linear regulators LR1, LR2 and LR3 are implemented as fast bipolar transistors (BJTs) and they are responsible for compensating the current ripple of the output inductor of the zeta converter. By sensing the output voltage, an operational amplifier (OpAmp) measures the difference between the output voltage and a reference and amplifies the error in order to generate an equivalent current for the base of the BJT. The current flowing through the collector-emitter terminals of the BJT is proportional to the base current and it has the same ripple amplitude of the output inductor with a phase angle of 180°. In this way, the current trough the load is an addition of the output inductor current of the zeta converter and the current flowing through the LR regulator, which has the opposite angle. Thus the resulting current in the load is an ideal ripple-free constant DC waveform.

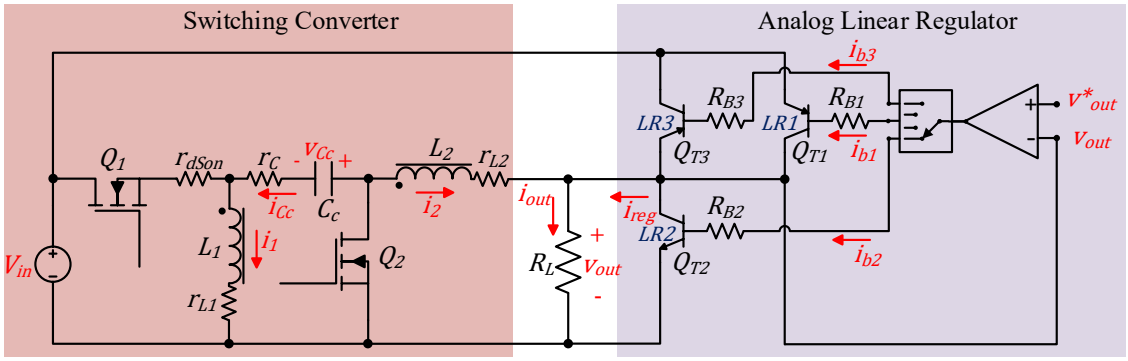

Fig. 1: Linear-assisted zeta converter.

Note that just one LR is operating at one time. The decision upon which LR is operating follows the rules below:

- LR1 is active when the input voltage is greater than the output voltage and the current flows from the input voltage source to the output through the BJT;
- LR3 is active when the output voltage is greater than the input voltage, thus the current flows from the output to the input through the BJT;
- LR2 is active when the input fluctuates around the output voltage in order to avoid switching among the linear regulators. In this case, one factor k can be associated to the output voltage in order to set the range of the input voltage in which the LR2 is active. Outside this range, the operation will fall in one of the previous cases.
- Optionally, LR2 can also be active when the input voltage is greater than the double of output voltage. In this case, it makes sense to dissipate power across LR2 since the V_{out} is less than the difference $V_{in} - V_{out}$, so the voltage across LR2 is smaller than the voltage across LR1.

To summarize the linear assisted operation, the following equation can be written to describe the rules above:

$$LR(ON) := \begin{cases} LR2, & (1-k)V_{out} \le V_{in} \le (1+k)V_{out} \\ LR1, & (1+k)V_{out} < V_{in} \le 2V_{out} \\ LR3, & V_{in} < (1-k)V_{out} \\ LR2, & V_{in} > 2V_{out} \end{cases} . \quad (1)$$

In order to allow a reliable design based on the static analysis, it is necessary to obtain a mathematical model of the overall topology. First, the model of the zeta converter without output capacitor is obtained and then the small signal model of the analog linear regulator circuit is obtained in order to determine how much output voltage of the OpAmp is necessary. The difference of this topology if compared to standard zeta converter topologies is that the influence of the linear regulator current has to be considered to obtain an approximate model for each switching mode of the switching converter. To do so, the influence of the linear regulator current is considered as an extra state, which substitutes the state regarding the output capacitor in conventional topologies.

Modeling of the zeta converter with influence of the linear regulator current.

The zeta converter preferably consists of an active switch Q_1, two magnetically coupled inductors L_1 and L_2, a passive switch D as a diode, and a small coupling capacitance C_c, which is much smaller than a comparatively smoothing capacitance at the output for suppressing the ripple of a switching regulator. In a synchronous topology, the diode is substituted by a MOSFET Q_2 that is synchronously driven with the high-side MOSFET Q_1. As long the topology is linear assisted, no output capacitor is employed. Thus, a state-space representation which describes the dynamical behavior of the topology can be obtained as follows.

The PWM zeta converter is a nonlinear dynamic system with structural changes over an operation cycle. If the converter is operating in the CCM, two switching modes are considered and the equivalent circuits belonging to each switching mode are given in Figure 2.

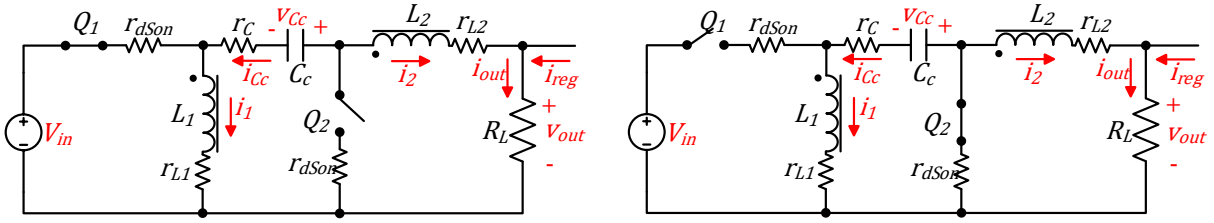

Fig. 2: Equivalent circuit when a) switch Q_1 is ON and b) switch Q_1 is OFF.

In the first switching mode, the dynamical equations can be obtained by applying the Kirchhoff's law in the circuit of Fig. 2.a). The state-space representation of the first switching mode of the zeta converter can be represented then, as

$$\begin{aligned} \mathbf{F}\dot{\mathbf{x}}(t) &= \mathbf{A_I}\mathbf{x}(t) + \mathbf{B_I}u(t) \\ \mathbf{y}(t) &= \mathbf{C_I}\mathbf{x}(t) \end{aligned} \tag{2}$$

where $\mathbf{x}(t) = [i_1(t) \quad i_2(t) \quad v_{Cc}(t) \quad i_{reg}(t)]^T$ is the state vector, $u = V_{in}$ is the input and the matrices are

$$\mathbf{A_I} = \begin{bmatrix} -(r_{dSon} + r_{L1}) & -r_{dSon} & 0 & 0 \\ -r_{dSon} & -(r_{dSon} + r_C + r_{L2} + R_L) & 1 & -R_L \\ 0 & -1 & 0 & 0 \\ r_{dSon} & (r_{dSon} + r_C + r_{L2} + R_L) & -1 & R_L \end{bmatrix}$$

$$\mathbf{F} = \begin{bmatrix} L_1 & M & 0 & 0 \\ M & L_2 & 0 & 0 \\ 0 & 0 & C_c & 0 \\ -M & 0 & 0 & L_2 \end{bmatrix}, \quad \mathbf{B_I} = \begin{bmatrix} 1 \\ 1 \\ 0 \\ -1 \end{bmatrix}, \quad \mathbf{C_I} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}. \tag{3}$$

In a very similar way, the state space representation for the second switching mode can be obtained by applying the Kirchhoff's law in the circuit of Fig. 2.b). Thus, the state-space representation of the second switching mode becomes

$$\begin{aligned} \mathbf{F}\dot{\mathbf{x}}(t) &= \mathbf{A_{II}}\mathbf{x}(t) + \mathbf{B_{II}}u(t) \\ \mathbf{y}(t) &= \mathbf{C_{II}}\mathbf{x}(t) \end{aligned} \tag{4}$$

where the matrices are

$$\mathbf{A_{II}} = \begin{bmatrix} -(r_{L1} + r_C + r_{dSon}) & -r_{dSon} & -1 & 0 \\ -r_{dSon} & -(r_{dSon} + r_{L2} + R_L) & 0 & -R_L \\ 1 & 0 & 0 & 0 \\ r_{dSon} & (r_{dSon} + r_{L2} + R_L) & 0 & R_L \end{bmatrix},$$

$$\mathbf{B_{II}} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad \mathbf{C_{II}} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}. \tag{5}$$

Note that the mutual inductance M from the coupled inductors appears in the state-space representation of both switching modes. The mutual inductance is related to the coils inductances by

$$M = h\sqrt{L_1 L_2}, \tag{6}$$

where h is the coupling coefficient, which consists of a value between 1 (perfectly linked inductors) and 0 (uncoupled inductors), due to the flux lines that do not cut through the coupled inductor completely.

One can see that there is a fourth differential equation, which is used to express the influence of linear regulator dynamics into the zeta converter conventional model. As mentioned earlier, the linear regulator current i_{reg} is just used to compensate the current ripple of the output inductor of the zeta

converter. This means that dynamical equation of the linear regulator circuit can be simply represented as the opposite of the dynamical equation of the output inductor L_2 current, i.e.,

$$\frac{di_{reg}(t)}{dt} = -\frac{di_2(t)}{dt}. \tag{7}$$

The equations (2) and (4) are used to describe the dynamical behavior of the linear-assisted zeta converter and they can be used later for average modeling and control purposes. It is not in the scope of this work to provide the average model and to analyze the dynamical response of the proposed topology.

Modeling of the linear regulator circuit.

In order to determine the output voltage of the OpAmp, which provides the base signal for the BJT, the small signal model of the block (OpAmp+BJT) has to be analyzed. When LR2 is active the equivalent model is given in Fig. 3, where an NPN BJT is employed. The BJT is represented by the so-called hybrid Pi model and the OpAmp is modelled as shown in the figure. When operating in active region, the transistor adjusts the collector current i_C to be β times the base current i_B. In addition, the linear regulator current can be related to the base current of the BJT by the following expression,

$$i_{reg}(t) = -i_C(t) = -\beta i_B(t). \tag{8}$$

The BJT base voltage V_B can also be expressed as

$$V_B = V_E + V_{BE}, \tag{9}$$

where V_E is the emitter voltage of the BJT, which is connected to the ground, and V_{BE} is the voltage drop of the internal diode connected between the base and emitter. In addition, the base voltage V_B of the BJT can be related to the output voltage of the amplifier V_{amp} by

$$V_{amp}(t) = V_{BE} - \frac{R_B}{\beta} i_{reg}(t) \tag{10}$$

Differentiating both sides of the equation above, one has

$$\frac{dV_{amp}(t)}{dt} = -\frac{R_b}{\beta}\frac{di_{reg}(t)}{dt}. \tag{11}$$

Thus, the rate in which the output voltage of the OpAmp changes is the same rate which the LR current changes multiplied by a factor of R_B/β. Equation (11) is used to predict the output voltage of the amplifier. This allows to determine in advance the required supply voltage of the OpAmp, which has to be greater than V_{amp}^{max}.

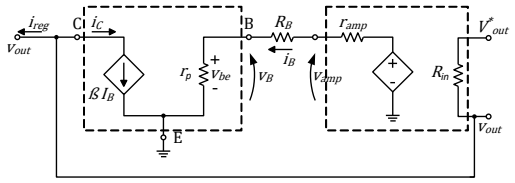

Fig. 3: Small signal model of the LR circuit when LR2 is active.

The OpAmp output voltage is calculated in a different way when LR1 and LR3 are active. These two linear regulator paths use PNP BJTs, so the V_B is expressed as

$$V_B = V_E - V_{BE}. \tag{12}$$

When LR1 is active, the emitter is connected to the input voltage, so in this case $V_E = V_{in}$, as shown in Fig. 4.a and, when LR3 is active, the emitter is connected to the output voltage, so $V_E = -V_{out}$, as shown in Fig. 4.b. This means that the OpAmp output voltage, when the LR1 is active, can be expressed as

$$V_{amp} = V_{in} - V_{BE} - \frac{R_B}{\beta} i_{reg}, \tag{13}$$

and, when LR3 is active, the OpAmp output voltage is

$$V_{amp} = -V_{out} - V_{BE} - \frac{R_B}{\beta} i_{reg}. \tag{14}$$

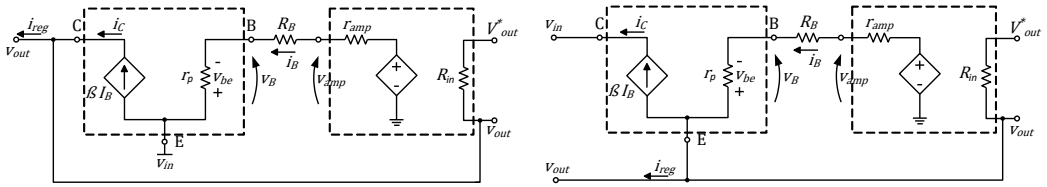

Fig. 4: Small signal model of the LR circuit when a) LR1 is active and b) LR3 is active.

Design example and simulation

The operation of the zeta converter is described as follows. The coupling capacitor C_c is charged to V_{out} in steady-state. When the switch Q_1 is ON, the coupling capacitor C_c, previously charged to V_{out}, is connected in series with L_2 and the both inductors L_1 and L_2 are charging. The voltage in the primary inductor is $V_{L1} = V_{in}$ and the voltage across the secondary inductor is also $V_{L2} = V_{in}$, because the winding ratio of the coupled inductor is 1:1. During this period, the switch Q_2 is closed and sees a voltage of $V_{in} + V_{out}$.

When the switch Q_1 is OFF and Q_2 is ON, the primary inductor L_1 is discharged through the coupling capacitor and ground. The secondary inductor L_2 is also discharged, while providing power to the load. So the voltage across the opened MOSFET Q_1 is $V_{in} + V_{out}$. In this state, the primary inductor is in parallel with the C_c. Thus, the voltage across L_1 is $V_{L1} = -V_{Cc} = -V_{out}$ and the secondary inductor experiences also a voltage of $V_{L2} = -V_{out}$.

By the Volt-Second Balance principle, the DC transfer function of the zeta converter can be found, as follows

$$\frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{D_c}{1 - D_c} \tag{15}$$

For a duty cycle D_c lower than 50%, the zeta performs as a buck converter, and for D_c higher than 50%, as the boost converter. The maximum duty cycle D_c^{max} occurs at V_{in}^{min} and minimum duty cycle D_c^{min} occurs at V_{in}^{max}. In order to design the zeta converter, the requirements are previously determined as shown in Table I.

Table I: Requirements for the zeta converter design.

	Parameter	Value
Minimum input voltage	V_{in}^{min}	3 V
Maximum input voltage	V_{in}^{max}	20 V
Output voltage	V_{out}	5 V regulated, 7 V unregulated
Output power	P_{out}	2 W
Switching frequency	f_s	350 kHz

Selecting passive components

One of the first steps in designing any switching converter is to decide how much inductor ripple current Δi_L to allow. First, the input current, which is higher when the duty cycle is maximum, i.e., at V_{in}^{min}, is calculated as follows

$$I_{in} = \frac{P_{out}}{V_{out}} \frac{D_c^{max}}{1 - D_c^{max}} = 0.667\ A \tag{16}$$

Furthermore, a maximum efficiency of $\eta = 90\%$ can be considered, thus the input current is increased by a factor of

$$I'_{in} = \frac{I_{in}}{\eta} = 0.741\ A \tag{17}$$

Hence, a rule of thumb is to allow 10 to 40% ripple in the inductor current. However, considering the voltage drop in the linear regulator of $V_{LR} = 13\ V$ in the worst case, the output inductor current ripple has to be small enough in order to result in less power dissipated in the LR afterwards. Thus, considering a ripple of 1.3%, the allowed current ripple is

$$\Delta i_L = 0.741 \times 1.3\% = 0.0096\ A \tag{18}$$

In an ideal, tightly coupled inductor, with each inductor having the same number of windings on a single core, the mutual inductance forces the ripple current to be split equally between the coupled inductors. The inductance required in a coupled inductor is, then, estimated to be the half of what would be needed if there were two separate inductors, as follows

$$L_1 = L_2 = \frac{1}{2}\frac{V_{in}^{min}\, D_c^{max}}{\Delta i_L\, f_s} = 312\ \mu H \tag{19}$$

The coupling capacitor must handle the output voltage ripple which is dependent on the output current ripple. In this topology, the load is connected in series with the output inductor. Considering the inductor current fully flowing in the load (disregarding the LR path), the output voltage ripple can be calculated as follows,

$$\Delta V_{out} = \Delta V_{Cc} = \Delta i_L \frac{V_{out}^2}{P_{out}} = 0.236\ V \tag{20}$$

Finally, the coupling capacitor can be calculated by the following equation

$$C_c = \frac{D_c^{max}\, I_{out}}{\Delta V_{Cc}\, f_s} = 2.422\ \mu F. \tag{21}$$

Selecting active components

Next step is to select the active components, i.e., two MOSFETS, in case the synchronous topology is used. In this paper, the synchronous topology is considered and the MOSFETs must handle the peak current given by

$$I_{FET(PK)} = I_{in} + I_{out} + \Delta i_L = 1.03\ A \tag{22}$$

As discussed earlier, when not conducting, the MOSFETs experience a voltage of $V_{in}^{max} + V_{out}$. So the rating voltage has to be above this value. Finally, the components can be selected from the market, and the real parameters are chosen to be as close as possible to the theoretical values. Table II shows the selected components for the real circuit implementation.

Table II: Selected components for the real circuit implementation.

Component	Real Values	Part number
Coupled inductor	$L = 330\ \mu H$, $DCR = 0.367\ \Omega$	MSD1514
Coupling capacitors	$C_c = 3 \times 1 \mu F$, $ESR = 0.05\ \Omega$	Ceramic capacitors
MOSFETs	$R_{ds(on)} = 10\ m\Omega$, $V_{DS} = 80\ V$, $I_D = 40\ A$	IPA1000N08N3
NPN BJT, PNP BJT	$V_{CEO} = 40\ V$, $I_C = 600mA$	SST4401, SST4403
Operational amplifier	$V_{supply} = \pm 4.5$ to $\pm\ 16\ V$	LT6274
MOSFESTs controller	-	LTC4442

Simulation results

In order to simulate the circuit with the parameters of Table II, the spice models of the components were used. The circuit is simulated considering just the first case of the LR operation, i.e., the input voltage is less than the output voltage and LR1 is active. This is the case where the input current is higher, so it can be considered the worst case. The circuit implementation on LTSpice is shown in Fig. 5. Note that three ceramic capacitors of 20nF each were included in the output of the zeta converter. These ceramic capacitors are used to suppress high frequencies noise, so the results are better visualized.

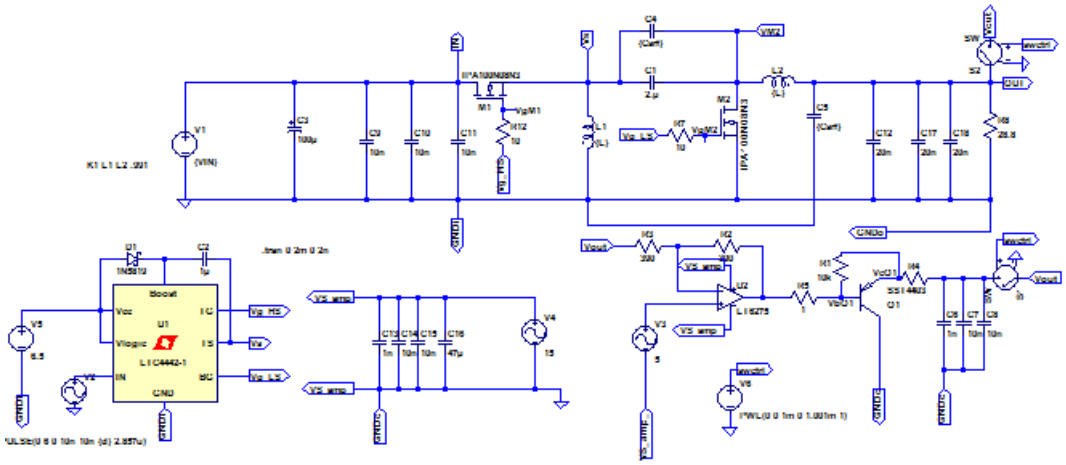

Fig. 5: Circuit implementation on LTSpice when LR1 is operational.

Fig. 6 shows the input and output voltages waveforms. The input is $V_{in} = 3V$ and the output is about $V_{out} = 6.4\,V$, when the linear regulator is not operational (before 1ms). Note that, at 1 ms the LR starts operating and the output voltage is regulated to approximately $V_{out} = 5.4\,V$. As long as the closed loop operation of the zeta converter is not considered in this paper, it is not necessary to regulate the output voltage by controlling the switches of the converter. In order to have current flowing from the output to the input through the LR, the zeta converter has to provide more current to the output. One way to do that, is to set a reference voltage for the LR smaller than the zeta converter is able to provide in a desired operation without LR, which is $V_{out} = 6.4\,V$. Thus, the reference voltage of the LR was set to be $V_{LR}^{ref} = 5\,V$. Note that after 1 ms, the output voltage ripple is almost completely suppressed. This is due to the linear regulator that is compensating the current ripple as it will be shown.

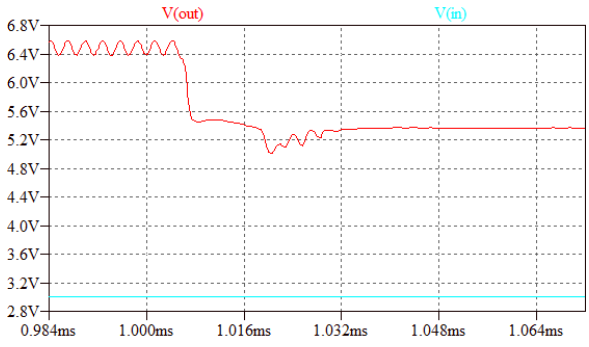

Fig. 6: Output voltage with output small ceramic capacitors.

After the LR starts to operate, the current ripple of the output inductor is compensated by the LR, as shown in Fig. 7. So the current ripple in the load is compensated without any auxiliary electrolytic capacitance. A zoom in of Fig. 7 is provided on the right, where the current compensation by the LR can be seen in detail. By subtracting the LR current Ie(Q1) from the output inductor current I(L2), one sees exactly the very small ripple load current I(R8), depicted in Fig. 8.

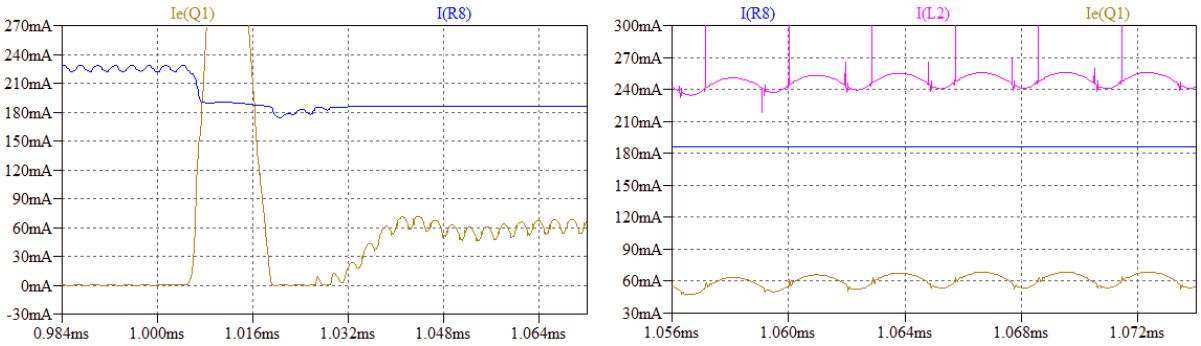

Fig. 7: Ripple compensation by the LR. I(R8) is the current in the load, I(L2) is the secondary inductor current and Ie(Q1) is the LR current.

The small ripple characteristics are seen again in Fig. 8. The output voltage has ripple of approximately $\Delta V_{out} = 7\ mV$ and the load current has ripple of approximately $\Delta i_{load} = 200\ \mu A$. These values are much smaller if compared to the values of $\Delta V_{out} = 200\ mV$ and $\Delta i_{load} = 10\ mA$, respectively, in the case where the LR is not operational.

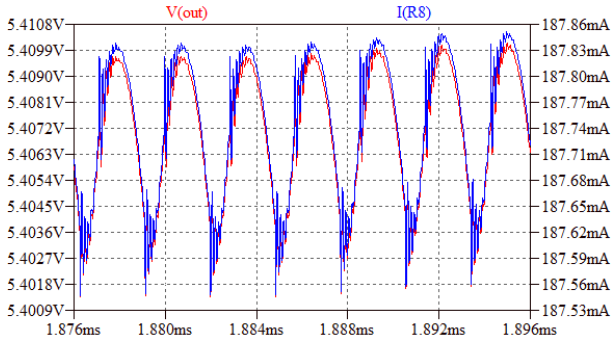

Fig. 8: Output voltage ripple and load current ripple.

Experimental results

In order to confirm the simulation results, a linear assisted zeta converter was built. The setup is shown in Fig. 9. It consists of the main (zeta) switching converter and three linear regulators. Some electrolytic capacitors are placed in order to stabilize the input sources, but no electrolytic capacitors are used at the output. The output and gate driver voltages are shown in Fig. 10 on the left. After some time, the LR starts operating and the output voltage is regulated to about 5 V. Due to realistic parasitics, the voltage ripple is not completely compensated, however is much reduced as shown. On the right side of Fig. 10, the output and the LR currents are presented. The output current ripple is reduced when the LR starts operating, which emphasizes the ripple compensation of the proposed topology.

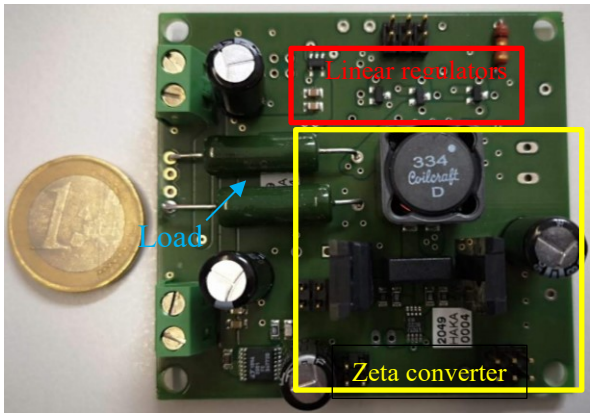

Fig. 9: Linear-assisted zeta converter experimental setup.

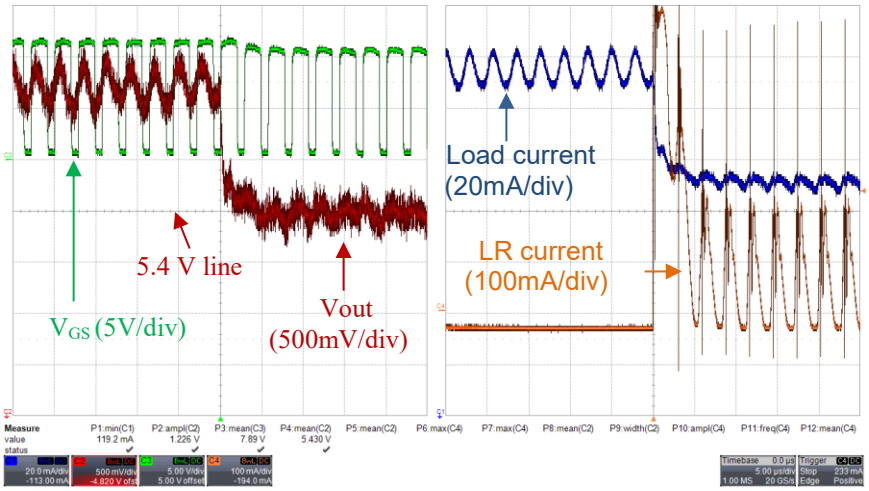

Fig. 10: Experimental results of the real implementation circuit.

Conclusion

This paper presented the modeling and design of a linear-assisted zeta converter. In order to reduce the output voltage ripple of the main (zeta) converter without employing electrolytic capacitor, a parallel scheme with a linear regulator is used. The zeta converter is modeled similar to the conventional topology, except the fact that the linear regulator is modeled as an extra state which substitutes the output capacitor voltage state in a conventional topology. The new state is modeled as the opposite of the output inductor current, in order to cancel the ripple in the output. The design of the proposed converter is presented in details and static operation of the overall system is simulated, where the Spice models of each component is considered. Although the dynamics equations are presented in this paper, the dynamical behavior or control considerations are not taken into account. These topics will be discussed further in a future work. The impact of parasitics converter will also be studied in order to improve the ripple compensation. Thus, this paper focused on showing the operation of the linear-assisted zeta converter, where the topology was simulated and validated with experimental results.

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