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PILOT-LINE PROCESSING OF VERY LARGE (21 X 21 CM²) AND THIN MC-SI SOLAR CELLS

Florian Clement[1], Ralf Preu[1], Isolde E. Reis[1], Daniel Biro[1], Jochen Rentsch[1], Martin Zimmer[1], Stefan Rein[1], Gernot Emanuel[1], Alexander Krieg[1], Armin Müller[2] and Frank Martin[2]
[1]Fraunhofer Institute for Solar Energy Systems (ISE), Heidenhofstrasse 2, 79110 Freiburg i. Brsg., Germany
Phone: +49 (0)761–4588–5479, Fax: +49 (0)761–4588–9250, e-mail: florian.clement@ise.fraunhofer.de
[2]Deutsche Solar AG, Berthelsdorfer Straße 111 A, 09599 Freiberg/Sachsen, Germany

ABSTRACT: Enlargement of the wafer size from 15.6 x 15.6 cm² to 21 x 21 cm² seems to be an effective cost reduction strategy of solar cell production. Especially batch-type production shows a high cost reduction potential. First cell manufacturers are already able to produce multi-crystalline (mc) solar cells based on very large scale (VLS) wafers. But before a mass production is worth, a few challenges like mechanical yield during cell manufacturing and homogeneity over total wafer surface have to be solved. Therefore, more than 100 VLS solar cells with a thickness of max. 240 µm were processed at the pilot-line of the **P**hoto**V**oltaic **T**echnology **E**valuation **C**enter (PV-TEC) at the Fraunhofer ISE. To transfer the standard solar cell process successfully, a front grid optimisation was carried out, which resulted in cell efficiencies up to 15.2%. Compared with standard 15.6 x 15.6 cm² mc solar cells the efficiency is in the same range. Furthermore, two mini-modules were successfully produced.
Keywords: Sizing, Multi-Crystalline, Manufacturing and Processing

1 INTRODUCTION

Reducing costs per W_p at low economical risks is a major goal of research and development in crystalline silicon solar cell production technology. Therefore, technologies close to the state of the art are favourable for low economical risk of R&D. Reducing the costs can be mainly addressed by efficiency increase, silicon material and production cost reduction. For the latter three different options are possible. First, low-cost silicon material can be used, while it remains a challenge to maintain the efficiency of the solar cells. Second, thinner wafers reduce the use of wafer material and also the demands on the carrier lifetime of the cell. Third, larger wafers are reducing the production costs per W_p significantly due to lower silicon loss in wafer manufacturing, higher production capacity, less handling steps per W_p and higher packing density in the module.

For batch-type production lines a cost reduction up to 20% compared with 12.5 x 12.5 cm² wafers is possible assuming that all production and cell values are the same. Even for lower efficiencies (up to 13%) and mechanical yields (down to 90%) a cost reduction is reachable [1, 5].

But, in times of silicon shortage the actual trend goes to thinner wafers instead of larger wafers. However, if the silicon feedstock bottleneck will be overcome, the very large scale (VLS) solar cell format might become more interesting for industry again. Hence, pilot-line processing of VLS (21 x 21 cm²) and thin (≤ 240 µm) solar cells is a promising way to go. Furthermore, first results show a very high potential for those cells [3, 4, 5].

The VLS multi-crystalline silicon wafers were produced by the Deutsche Solar. The material was melted and crystallized in the same crucible (combination of Bridgman and HEM technology).

2 FRONT GRID OPTIMISATION

The optimisation of the front contact grid for VLS solar cells is an important challenge. Earlier simulations and experiments show that a design with more than two bus bars is favourable [4,5].

In Table I the results of a simulation of different front grid designs is presented. Therefore, "GridSim", a simulation program developed at Fraunhofer ISE, was applied. The program considers shading caused by the front grid (optical losses) as well as serial resistance losses appearing in the solar cell (electrical losses). The simulation is based on the expected current density and voltage at the maximum power point (MPP). The influence of the number of bus bars (BB) was simulated by keeping all the other parameters except the number of fingers constant. For each number of bus bars the optimum number of fingers was also simulated.

The simulation was performed with the following input parameters:

- Finger height (mean):	10	µm
- Finger width (mean):	130	µm
- Bus bar width:	2000	µm
- Bus bar height:	12	µm
- Finger resistance:	3.5×10^{-8}	Ωm
- Emitter sheet resistance:	50	Ω/sq.
- Contact resistance:	1×10^{-3}	Ωcm²
- Current density (MPP):	28.5	mA/cm²
- Voltage (MPP):	510	mV
- Solder points per BB:	20	

Table I: Results of the front grid simulation

	2 BB	3 BB	4 BB
Optimum number of fingers	92	81	77
Optical losses (%)	7.5	7.7	8.4
Serial resistance (Ωcm²)	0.8	0.6	0.5
Electrical losses (%)	4.4	3.3	2.8
Cumulative losses (%)	11.9	**11.0**	11.2

The design with three bus bars yields the lowest cumulative losses (marked in Table I), so it was chosen for cell processing. Hence, for three bus bars the highest cell efficiency is expected. However, an increased number of fingers (86) was realised in the experiment to take fluctuations in the printing step (for example finger interruptions) into account. In Figure 1 a picture of a VLS solar cell (front) is shown.

Figure 1: Picture of the front of a VLS 21 x 21 cm² solar cell with three bus bars (BB) and 86 fingers

3 EXPERIMENTS AND RESULTS

3.1 Transfer of the standard solar cell process to VLS wafers

First, a transfer of the standard process for industrially processed screen-printed solar cells to VLS (21 x 21 cm²) and thin (thickness ≤ 240 µm) wafers is necessary. Therefore, all process steps had to be adapted to VLS wafers. The used standard process flow is shown in figure 2. Multi-crystalline material (0.5-2 Ωcm) supplied by the Deutsche Solar Ag was chosen.

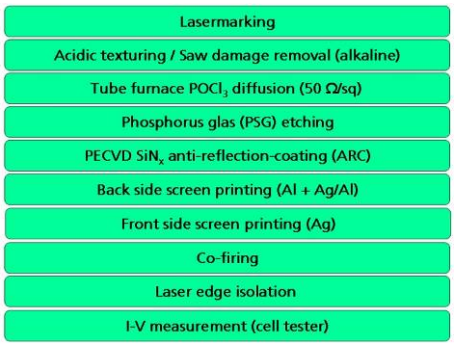

Figure 2: Process flow for VLS solar cells

The machines set up in the pilot-line of the PV-TEC meet all the requirements for industrial-like processing of up to 21 x 21 cm² wafers [2]. Only a few automation systems are not yet able to handle VLS wafers. Therefore, a few manual handling steps are necessary during the manufacturing process. Hence, the achieved mechanical yield of 90.5% is not as high as expected for industrially processing, but a good value for a first run.

Having a closer look at each process step, especially the co-firing in the fast firing furnace could be critical. Because for solar cells with an aluminium (Al) back surface field the influence of bowing due to mismatch of thermal expansion between silicon and aluminium is increased for larger and thinner wafers [3]. Therefore, it is necessary to use low-bow-pastes and furthermore to reduce the amount of Al-paste. By the use of such a low-bow-paste (amount of Al-paste in the second run: approx. 8 mg/cm²) it was possible to reduce the bow below 2 mm for all cells. Standard co-firing conditions (set point peak temperature: 860-920°C) were used. Alternatively the full area Al-contact on the rear could be replaced by a grid shaped metal contact with an additional dielectric passivation [3].

Furthermore, the optimum co-firing temperature for VLS solar cells is expected to diverge from the standard temperature due to the bigger thermal mass of VLS solar cells. In figure 2 the measured wafer peak temperatures of VLS and 15.6 x 15.6 cm² solar cells (thickness: about 240 µm) during the co-firing process are shown for two different set point peak temperatures. The amount of Al-paste on the back was approx. 8 mg/cm² for all measured wafers. The wafer temperature is 10-30 K lower for thin VLS solar cells. Therefore, the optimum co-firing set point peak temperature of the furnace should be approx. 20 K higher for VLS cells compared with 15.6 x 15.6 cm² standard solar cells.

All I-V measurement (STC) are performed using a flash light illumination of an automated cell tester.

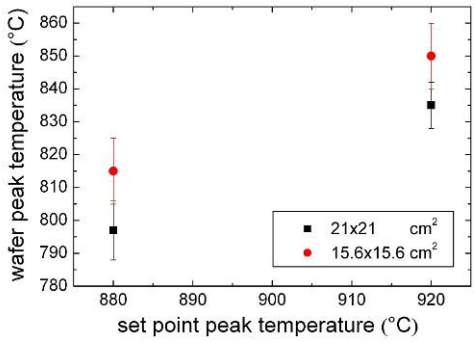

Figure 2: Measured peak temperatures of VLS and 15.6 x 15.6 cm² solar cells during the co-firing process

3.2 Cell results

In this work approx. 120 VLS solar cells (thickness ≤ 240 µm) of the same material were produced and characterised. The first run (≈ 60 cells) was made to evaluate the optimum process parameters, for example the best co-firing peak temperature. Therefore, the cells were split into 10 groups: 5 different peak temperatures were used for textured as well as untextured cells. In the second run all cells (≈ 60 cells) were fabricated with the optimum process parameters evaluated in the first run.

In figure 3 the mean fill factors of the first run are plotted against the set point peak temperature of the co-firing furnace. The highest fill factors were achieved for set point peak temperatures of about 880-900°C. The pretty high value for the fill factor (>78%) indicates that a good contacting process was realised. Optical measurements of the front finger grid confirm that the printing step was very successful. Mean finger heights of 10-12 µm and finger widths of about 130 µm were measured. The estimated input parameters for the simulation of the front grid (see table I) are confirmed. Furthermore, almost no finger interruptions can be observed (q.v. figure 1).

In figure 4 the mean short circuit currents J_{SC} of the first run are plotted against the set point peak temperature of the co-firing furnace. An increase in current of approx. 3% is shown by the use of acidic texturation. Hence, textured cells were used in the second run.

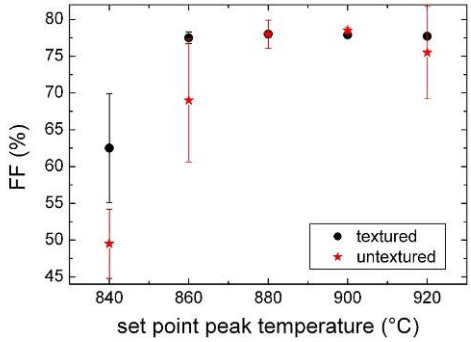

Figure 3: Mean fill factors of textured and untextured VLS solar cells for different set point peak temperatures in the first run

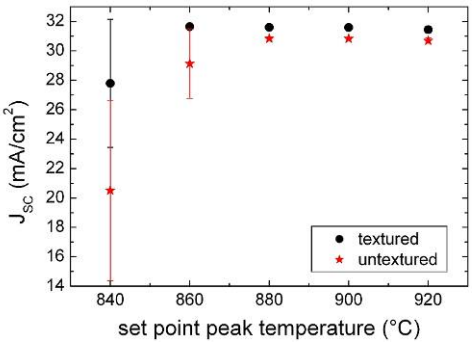

Figure 4: Mean short circuit currents of textured and untextured VLS solar cells for different set point peak temperatures in the first run

Considering the results for textured cells from the first run 880°C was chosen as optimum set point peak temperature. The distribution of the achieved efficiencies over all cells is shown in figure 5 (left). A spreading of the efficiency between 10 and 15.5% is observed. A comparable spreading is also observed for the fill factor. That means that the pretty good values of the first run can be confirmed, but that a process instability exists.

To locate the instability, serial resistance (R_S) measurements were made. The results are shown in figure 5 (right). The same spreading as in the efficiency distribution (see figure 5 (left)) could be observed. Low (high) values for R_S result in high (low) fill factors and thus efficiencies. Generally, there are three main reasons for a high value of R_S:

- high emitter sheet resistance
- high contact resistance
- high serial resistance in the contacts

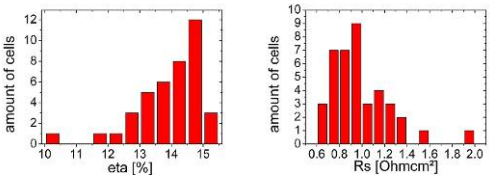

Figure 5: Distribution of the efficiencies (left) and R_S-values (right) in the second run

A high or inhomogenously distributed emitter sheet resistance can be excluded because sheet resistance measurements after the diffusion show a value of approx. 50 Ω/sq. very homogenously distributed over the cell. A high serial resistance in the front finger grid can also be excluded. Optical measurements show that almost the same finger geometry as in the first run was realised. Furthermore, the same front side paste was used in both runs.

Consequently, a high contact resistance could be the reason for the high R_S-values. To verify this assumption CoRReScan (contact resistance scan) measurements were done [6]. In figure 6 the results of two VLS cells are presented: one cell with a low R_S-value and one with a high R_S-value. The distribution of the contact potential V_C between the fixed contact needle on the grid and the scanning measurement probe is shown. If problems with the emitter sheet resistance can be excluded a high measured contact potential is related to the contact resistance. Therefore, it is clearly shown that the high R_S-values result from a very high contact resistance and that the high contact resistance is the reason for the fluctuation of the fill factor and thus of the efficiency in the second run.

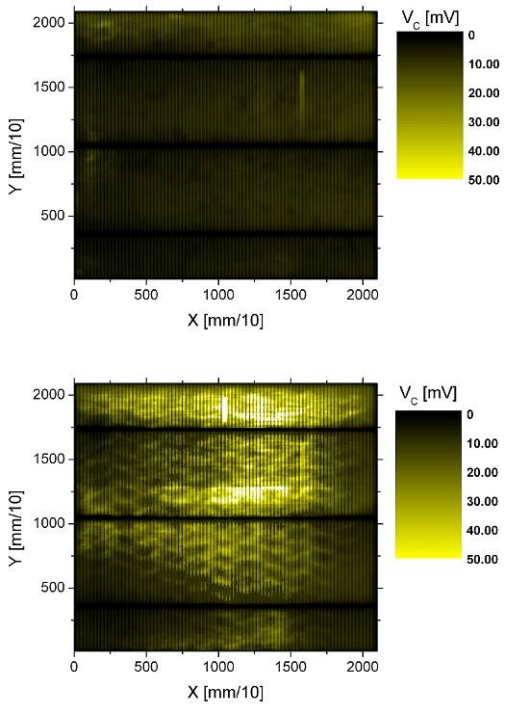

Figure 6: CoRReScan- measurements of a VLS cell with a low R_S-value (top) and with a high R_S-value (bottom)

The technological reason for the fluctuations in the second run could be a minor deviation from the optimum peak temperature in the co-firing process. The big difference in the contact resistance of equally processed cells and the visible belt structure (see figure 6) is typical for such a deviation. An explanation could be the fact that there was a small modification in the standard co-firing process between the two runs.

Nevertheless the best results of the second run confirm the good results from the first run. In table II the results of the I-V measurements from the first and second run are summarised.

Table II: Results of IV-measurement of VLS cells.

	first run		second run	
	mean	best	mean	best
Amount	5	1	40	1
V_{OC} [mV]	610±1	611	606±1	607
J_{SC} [mA/cm²]	31.6±0.2	31.7	31.5±0.3	31.7
FF [%]	78.0±0.3	78.3	72.7±5.0	78.4
η [%]	15.0±0.1	15.2	13.9±1.0	15.1

Finally, there is the question if the cell process was homogenous over the whole cell surface. Therefore, a SR-LBIC (spectral response – light beam induced current) measurement of a VLS solar cell was made and is shown in figure 7. A reasonable homogenous diffusion length distribution over the whole cell area (except the 3 bus bars) was determined. Only in small regions, mainly near the left edge, lower diffusion lengths can be observed. This indicates that either the material quality is low-graded in this regions or there are any bad influences during the cell process on the edges. However, the mean diffusion length over the whole cell is 288 µm, which is a quite good value for multi-crystalline material.

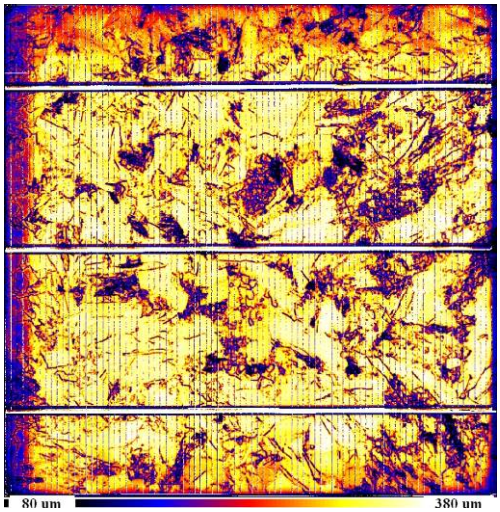

Figure 7: Diffusion length distribution of a VLS cell. The scale is in µm.

Table III: Results of IV-measurement of two VLS cell and mini-modules.

Cell ID	28		30	
	cell	module	cell	module
V_{OC} [mV]	610.0	608.9	610.0	608.5
I_{SC} [A]	14.0	14.3	14.0	14.3
FF [%]	77.9	70.5	76.9	70.7
η [%]	15.1	14.0	14.9	14.0
P_{MPP} [W]	6.65	6.15	6.57	6.15

3.3 Results of mini-modules

To prove the concept of VLS solar cells for the module technology, two 25 x 25 cm² mini-modules (one cell per module) were produced with standard tabbing, soldering and laminating technology. Because of the high current of the textured cell (about 14 A), tabbing material with a thickness of 200 µm (width = 2 mm) was used. The results of I-V measurements of the two cells and fully illuminated mini-modules are presented in table III. On the one hand a fill factor drop of about 6-7% absolute due to serial resistance losses in the module is observed. On the other hand a current gain of approx. 2-3% due to additional collected light mainly in the white regions besides the cell is measured. This current gain was confirmed by measurements where the white regions were shaded. However, a module efficiency of 14% (cell area was used for calculation) was reached, which is a pretty good value for a module-prototype of a VLS solar cell.

4 CONCLUSIONS

Very large scale (VLS) solar cells show in principle a great cost reduction potential by the use of batch-type production lines. But in times of silicon shortage the cost savings for producing thinner cells are higher than for producing larger ones. However, the situation could change in the near future and a demand for VLS solar cells could emerge abruptly.

In our experiments it was shown that pilot-line production of VLS solar cells with a mechanical yield over 90% is possible under standard conditions without any changes in the process flow. Cell efficiencies up to 15.2% were reached for VLS multi-crystalline solar cells In a second run (same material) the good results were confirmed. The strong differences especially for the fill factors in the second run can be explained by high values of the contact resistance caused probably by a non-optimum co-firing process. However, compared with 15.6 x 15.6 cm² solar cells the efficiencies are in the same range. Furthermore, a quite good homogeneity over the whole cell area was achieved with our pilot-line process.

Finally, first mini-modules were produced and measured. A module efficiency of 14% was achieved. This shows that modules of VLS solar cells could be successfully produced under standard conditions.

5 ACKNOWLEDGEMENTS

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