ALL-SCREEN-PRINTED 120-µM-THIN LARGE-AREA SILICON SOLAR CELLS APPLYING DIELECTRIC REAR PASSIVATION AND LASER-FIRED CONTACTS REACHING 18% EFFICIENCY

Luca Gautero[1], Marc Hofmann[1], Jochen Rentsch[1], Anke Lemke[1], Sebastian Mack[1], Johannes Seiffe[1], Jan Nekarda[1], Daniel Biro[1], Andreas Wolf[1], Bernd Bitnar[2], Jean-Michel Sallese[3], Ralf Preu[1]

[1]Fraunhofer Institute for Solar Energy Systems (ISE), Heidenhofstrasse 2, D-79110 Freiburg, Germany

[2]SolarWorld Innovations GmbH, Berthelsdorfer Str. 111 A, D-09599 Freiberg, Germany

[3]Ecole Polytechnique Fédérale de Lausanne, 1015 Lausanne – Switzerland

ABSTRACT

The market need for a lower price per $Watt_{peak}$ asks for the development of solar cell designs with a low production cost and a high performance. An approach to reach a high efficiency with a solar cell structure containing a diffused emitter on a p-type silicon wafer is the implementation of a PERC structure on the rear side [1]. This structure gets advantageous to the standard screen printed solar cell when its production cost stays comparable to the latter and offers a higher efficiency [2]. Since this technique can inherently be applied to thinner wafers, an additional advantage comes from the reduced material consumption. The purpose of this work is to introduce a production sequence able to create a PERC structure on thin silicon wafers using steps available in the PV industry or at least close to industrial application. Applying this process on Czochralski (Cz) wafers of 120 µm thickness, a stable efficiency of 18.0 % was achieved

INTRODUCTION

The recent social developments and debates on energy generation from renewable energies is pushing one of the most established one, photovoltaic, to confront on the cost scale with traditional fuel energy sources. The result is a strict demand of cost reduction.

From published studies [2], a roadmap towards lower production cost features higher production volumes, higher efficiency silicon solar cells with respect to conventional present technology and lower silicon wafer thickness was delineated, this work addresses the two latter challenges proposing an optimized process sequence.

Considering simply the increase of the ratio surface to volume, it is easy to understand the increased importance of surface passivation. The advantage of an all surface passivated scheme is an increased blue and red response. Both front side and rear side were optimized and a special focus on the rear surface structuring is described in this paper.

The use of conventional metallization processes, namely screen print, and the conjoint work of an industrial partner for specific steps in the process flow highlights the technology transfer value of the experiment.

EXPERIMENTAL

The solar cells for the experiment have been fabricated using 1500 thin mono-crystalline CZ wafers (2 Ωcm p-type,125x125 mm^2, pseudo-square (diameter: 150 mm), thickness ~140 µm). Front-end processing steps such as alkaline texturing, three types of $POCl_3$ diffusion over the whole batch for emitter formation, phosphorus silicate glass removal and anti reflecting coating (ARC) deposition on the front have been performed at Deutsche Cell GmbH, Freiberg, Germany. Together with the thin silicon wafers group, a reference group of cells with a thickness of 210 µm has been processed and subsequently finished to as conventional solar cells including a full-area Alu-BSF rear using the standard industrial processing, the resulting average efficiency of 17.4% testifies the state of the art status of the front-end processing, this initial phase brings the cell thickness down to 130±5 µm. All steps thereafter have been conducted at Fraunhofer ISE, mainly within the pilot-line in the PV-TEC laboratory (PV-TEC) [3, 4].

One first task was to decide the best emitter between the proposed one would have been the suitable for the screen print road. Initial comparison of front side contact and blue response gave us the confirmation that a lower doping of the emitter would have still delivered a good contact and an increase in photo generated current due to a better response to short wavelength. The metallization of the front concentrates on fine line printing and subsequent silver plating, the advantage is a perfect emitter to finger contact formation during the firing of the Silver paste and reduced finger conductivity with the plating of silver.

The structuring of the rearside was most critical and therefore the most time consuming part of the experiment, several direct industrial deposition of dielectric were implemented on different sub-experiment, the results were affected by well known inversion channel shunting and the further effort were then concentrated on thin thermal oxide layer growth.

Contacting the cell with a laser pulse, a technique better known as laser fired contact (LFC) on a screen printed and fired Aluminum layer required the understanding of the process parameter influencing the contact quality, several contact tests lead to the optimal process window, more details on this subject will be published soon [5].

At the end of the several sub experiment we could add up all the successful implementation of the processes, in Figure 2 the optimized process flow of experiment is depicted. In the following a closer description of this process will be given.

As first step after front end processing, the emitter, present at the wafers rear surface, is wet chemically removed using an inline machine which exposes only the rear surface to a silicon etchant (nitric acid (HNO_3), hydrofluoric acid (HF) and DI water(H_2O)), after this first step the emitter is successfully removed and with a short hot dip (Potassium hydroxide (KOH) and H_2O) an evener surface can be prepared, for this second etching step the masking activity of the ARC is important to prevent parasitic etching of the front structure [6], namely the texture and the emitter.

Prior to a short wet oxidation step, the samples undergo a surface cleaning using a modified RCA clean [7, 8]; it includes a SC1 step (ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and H_2O) and a SC2 step (hydrochloric acid (HCl), H_2O_2 and H_2O), both followed by a dip in diluted HF acid, this is performed in a batch machine with full immersion using carrier able to host up to 100 wafers.

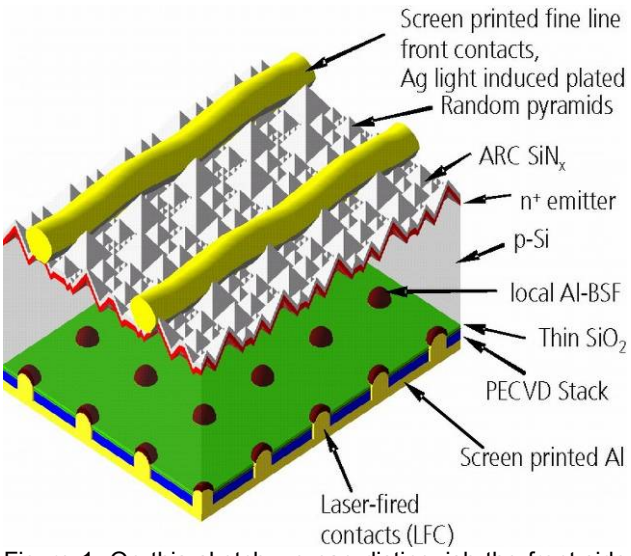

Figure 1. On this sketch we can distinguish the front-side with the two-step metallization and the rear surface structure with its application of a passivation stack and the LFC.

The silicon oxidation takes place in an industrial furnace, able to host as much as 200 wafers at a time; once again the masking of the ARC is crucial to prevent strong influences on the emitter profile [6] and to allow the formation of a thin thermal oxide only at the wafer rear side, where silicon is directly exposed. Immediately after a stack of capping dielectric layers has been deposited using an inline Plasma Enhanced Chemical Vapor Deposition system. This dielectric stack is composed by an hydrogenated amorphous silicon rich oxynitride (a-SiO_xN_y:H in short: SiriON [9]) layer and a dense hydrogenated amorphous silicon nitride (a-SiN_x:H, in short: SiN_x). The first is meant to act as a hydrogen reservoir and the second is intended to be a well reflecting layer for long wavelength radiation and to protect the passivation layers from any screen print paste action at high temperatures.

Figure 2. The process flow is depicted here. The processes performed at Deutsche Cell GmbH are highlighted in orange while in green the ones performed at Fraunhofer ISE are presented.

During the passivation steps it is possible to perform a first process control, the effective lifetime of the so far processed samples is measured (Table 1)

The metal pastes are applied with an adapted screen printing procedure that reduces the breakage of this seemingly stressful step for such thin wafers; this step has been influencing the yield in the first runs. Thin screen openings of 90 µm width were used without evident problems of finger interruption on the front side, the rear surface was covered with a low amount aluminum paste.

Using experience matured on the combination of front side paste and the thickness of the cells, we used a known

firing profile on an industrial inline implementation of a Fast Firing Oven (FFO). The rear contact vias were prepared using the LFC process [10]. Of high interest is the implementation of this technique on screen printed aluminum [5, 11]. The tool that was used for the implementation of this step can process one samples in few seconds, which is completely in agreement with the needs of a production line.

To cure the damage introduced by the sudden and local heating of the laser a short annealing step with a low temperature followed applying an inline belt furnace.

The final step, consisting in light-induced plating (LIP) takes place on an inline system. This step is meant to reinforce the conductance of the screen printed fingers. This machine needed some adjustments to handle correctly thin cells.

The cell structure resembles the one presented in Figure 1, with the additional thermal oxide layer in contact with the wafer rear side, capped by the PECVD layers. This approach features as highlight characteristic a passivation composed by silicon nitride and thermal oxide, and the metallization is entirely based on screen print, the process will be therefore mentioned in the following with the name of SiNTO SP.

PASSIVATION QUALITY AND PROCESS CONTROL

In order to control the status of the passivation during the further processing, four wafers were measured to investigate their lifetime during all steps before the metallization and after a Forming Gas Annealing (FGA) step, simulating the annealing performed before the silver plating (Table 1). The results show a strong increase of the quality, especially after the PECVD deposition, when hydrogen is suspected to fixate at the interface.

Table 1. To perform a process control the effective lifetime and the Implied-Voc are both monitored on four wafers. The average values, after the oxidation process and after the PECVD deposition process, are presented; these control cells also underwent a Forming Gas Anneal (FGA) in order to evaluate the full potential of the passivation.

effective lifetime (µs) @ $\Delta n = 5 \cdot 10^{14}$ cm^{-3}			
Sample	after oxidation	after PECVD	after FGA
Average -4-	17	62	68
Stdev	3	5	5
Implied V_{oc} (mV) @ illumination = 1 Sun			
Sample	after oxidation	after PECVD	after FGA
Average -4-	616	645	648
Stdev	4	2	2

A group of cells was monitored after metallization for their open-circuit voltage (V_{OC}) and, when possible, for their current versus voltage curve (IV meas.), in Table 2 one cell is presented as an example. The V_{OC} does not reach the level forecasted by the implied Open-Circuit Voltage (Implied-Voc) [12] values presented in Table 1, and the damage after the firing is not fully recovered.

Table 2. Monitoring of the open-circuit voltage (V_{OC}) during the processing, the small disagreement in V_{OC} between the SunsVoc tool and the IV measurement might be the result of a small spectral mismatch [13].

Cell B040	V_{oc} (V)	pFF	FF	η (%)	R_{Shunt} (Ωcm^2)
FFO (SunsVoc)	0.629	0.834			5220
Annealing (SunsVoc)	0.630	0.828			7170
Annealing (IV meas.)	0.633		0.76	17.8	
2nd Annealing (IV meas.)	0.633		0.75	17.8	

REFLECTANCE, EMITTER EVOLUTION AND METALLISATION

The thickness of the front side ARC during the chemical treatment was only reduced by few nanometers on the wafer edges, this was monitored by reflection measurements, and the local increase in weighted reflectance was around 0.4% absolute. This loss was recovered thanks to a thin deposition of SiN_x. This took place as a parasitic wrap around deposition while the rear surface stack was prepared in the PECVD machine. An absolute decrease of 0.3% in weighted reflectance was measured afterwards.

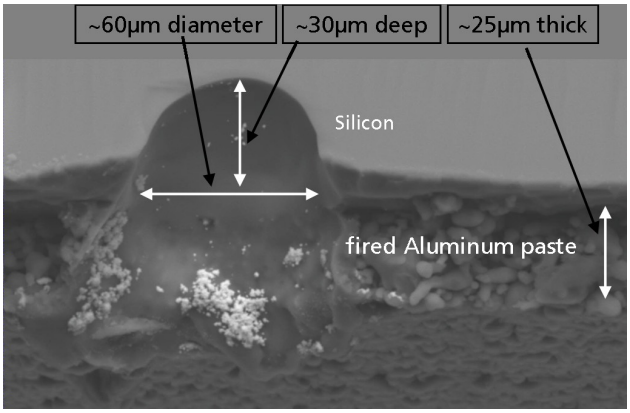

Figure 3. A section of the wafer is here shown, the sample is lightly tilted and we see perfectly the rear surface of the printed aluminum on the bottom of the picture, going up we see the printed and fired aluminum paste, the even surface, the LFC point and the silicon.

The front metallization was investigated by means of voltage drop from busbar to measured point, with the well known Correscan technique [14].

Analysis by means of scanning electron microscopy (SEM) indicated a growth of silver on top of the fingers of around 5 µm, this lead to a decrease of series resistance, resulting in an up to 10% higher fill factor (FF), this gain is compromised only by a 2% decrease in short-circuit current density(J_{SC}).

The amount of aluminum paste on the rear surface is no more related to the formation of a back surface field [15], therefore a lower amount of metal paste can be printed. Measurements have been performed with van der Pauws method to ensure that the conductance of this printed layer after firing was within acceptable ranges [16].

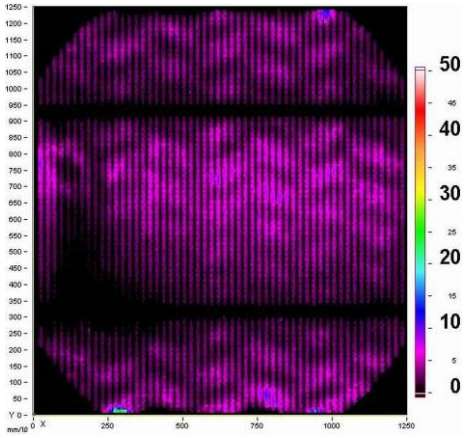

Figure 4. The picture shows a Corescan image indicating a low drop of voltage on the whole surface, the quality of firing process results homogeneous and the average value is within an acceptable range, below 10 mV.

The LFC process was optimized for a large surface contact and a minimal damage, in Figure 3 a SEM picture is giving us the geometrical data on such a metal contact configuration.

SOLAR CELLS RESULTS

Average results of solar cells processed with the optimized sequence in PV-TEC, are presented in Table 3 together with the best cell of the experiment, stabilization from the light induced degradation effect is also presented.

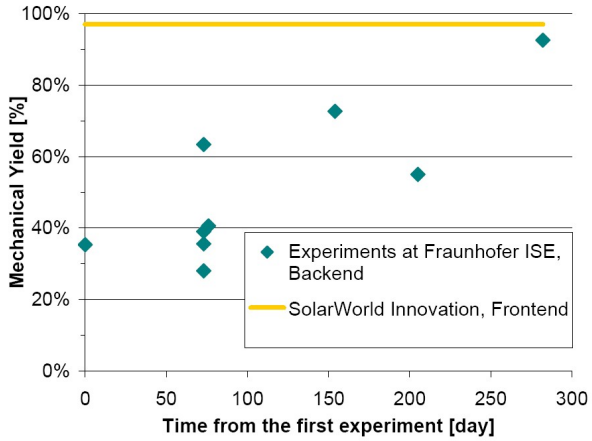

Figure 5. Like with every activity [17], the efficiency increases with time, and we can show here that a result above 90% has been achieved within this work.

Because of the dissociation of the Boron Oxygen complex, a trap level in the energy gap foster and give raise to recombination sites which decrease lifetime and therefore diffusion length, the thickness used in this work, like in previous work [18], enables a lower influence from of this decay and the final solar cell result is not affected as much as with standard thickness. This can allow the use of heavily doped base material, having benefits in both open circuit voltage and fill factor. The efficiency distribution curves are also presented (Figure 7).

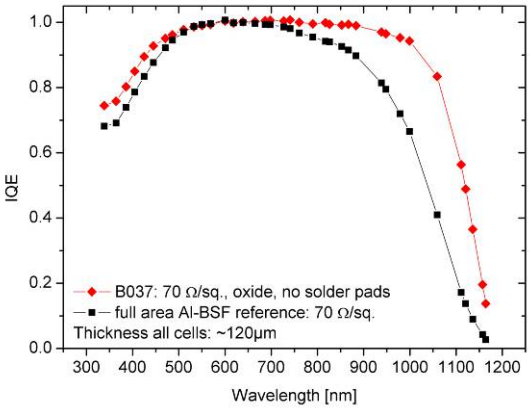

Figure 6. Comparison between two thin solar cells with two different rear surface structures, the Alu-BSF structure suffers from a reduced amount of Aluminum, which allowed the realization of the thin cell.

The small distribution of the results demonstrate the reproducibility of the process, the process implementation as demonstrated in the pilot line of PV-TEC can be quickly transferred to industry.

Table 3. Average values of the 24 cells group and best cell results, the material used was 2 Ω cm p-type Cz silicon.

	V_{OC}	J_{SC}	V_{mp}	J_{mp}	*FF*	η
Measurements on 24 solar cells	(mV)	(mA/cm²)	(mV)	(mA/cm²)	-	(%)
Median	636	37.0	520	34.4	0.76	17.8
average	632	37.0	514	34.2	0.75	17.6
Std. dev.	7	0.2	13	0.5	0.02	0.7
best cell (B067)	638	37.3	521	34.9	0.766	**18.2**
B067 Stabilized	636	37.3	520	34. 8	0.762	18.1
B067 Stabilized CalLab	635	37.3	521	34.6	0.760	18.0

In Figure 5 it can be seen that six experiments started in parallel, at that stage the different option for the passivation of the real were evaluated.

As mentioned before, over a time period of several months, groups of thin silicon wafers have been processed to investigate sensible aspects towards a best sequence, the yield of every experiment improved following a learning curve (Figure 5), assuming this work as a first proof of concept, the trend confirms feasibility.

One solar cell out of this process has been compared with a conventional industrial solar cell, featuring a full Aluminum coverage on the rear surface creating a back surface field; both cells had a thickness of about 120 µm, the comparison highlights the difference of the internal quantum efficiency. The gain of the SiNTO SP implementation over the Alu-BSF is more evident in the long wavelength region.

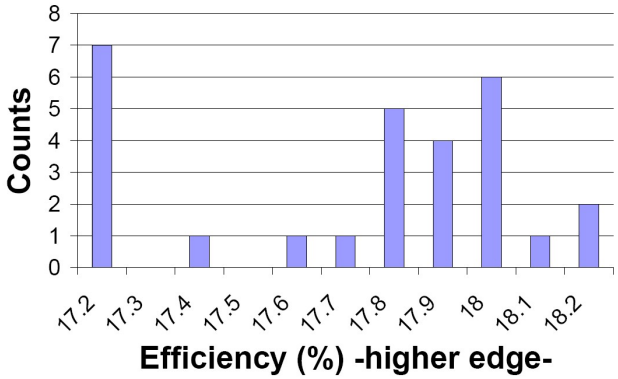

Figure 7. The bins of this histogram are 0.1% spaced and the higher edge is indicated, the first bin on the left collects all samples of the indicated efficiency and below.

A SEM image of a finished solar cell is presented in Figure 8; the surface to volume ratio is approximately doubled from a standard thickness cell.

OUTLOOK

From the comparison between the average Implied-Voc values in Table 1 and the measured V_{OC} values measured in Table 2 we notice that the damage introduced by the high temperature step is not yet entirely recovered, several are the possible causes. Focusing on the rear-surface structure, it could be pointed out that a more effective flattening of the rear surface would prevent the deposited layer to be discontinuous, i.e. where sharp edges are present. Increasing the density of the rear surface capping SiN_x would prevent interruptions of the passivation layer during the firing step.

The front side metallization could improve using thinner fingers, or even reduce the first metallization step to a seed printing step. This would lead to higher current density. Advanced metallization techniques [19] are now in development for the industrial application.

The cells did not exhibit any bowing.

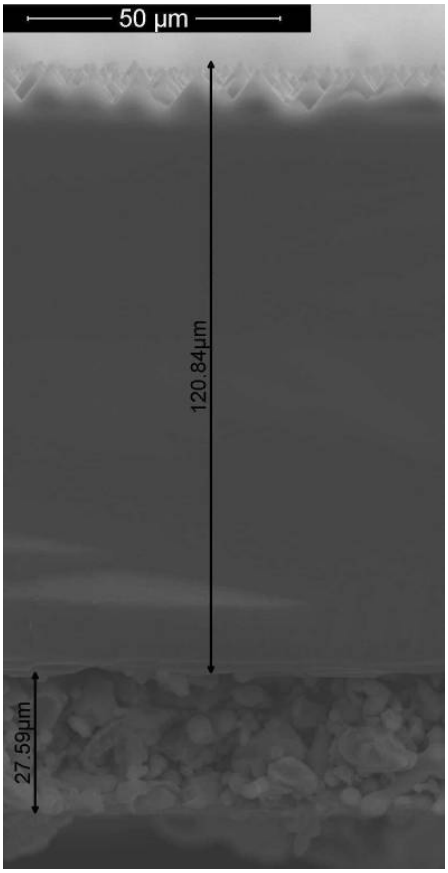

Figure 8. A picture of a complete section of the cell has been taken with a SEM, from this image it can be realized that the features like texture and metal layers begin to play a significant role on the total geometry of the cell at the thickness used in this work.

CONCLUSION

The fabrication of thin (130 µm) large area (125x125 mm^2) Cz silicon solar cells applying a LFC-PERC structure with stabilized top efficiencies of 18.0% is presented. The fabrication included the implementation of a thermal oxidation of the rear surface while the front was protected by the ARC. All process steps were performed using industrial or industrially applicable processes.

ACKNOWLEDGEMENT

This work has been supported by the European Project Crystal Clear under the contract number SES6-CT_2003-502583.

The authors would like to thank Deutsche Cell GmbH for the processing involved in the front end and all the team of PV-TEC for their effort towards the success of this work.

REFERENCES

[1] A. W. Blakers, A. Wang, A. M. Milne, J. Zhao, and M. A. Green, "22.8% efficient silicon solar cell," *Applied Physics Letters*, vol. 55, pp. 1363-5, 1989.

[2] C. del Canizo, G. del Coso, and W. C. Sinke, "Crystalline silicon solar module technology: towards the 1€ per watt-peak goal," *Progress in Photovoltaics: Research and Applications*, vol. 17, pp. 199-209, 2009.

[3] D. Biro, R. Preu, S. W. Glunz, S. Rein, J. Rentsch, G. Emanuel, I. Brucker, T. Faasch, C. Faller, G. Willeke, and J. Luther, "PV-Tec: Photovoltaic technology evaluation center - design and implementation of a production research unit," presented at Proceedings of the 21st European Photovoltaic Solar Energy Conference, Dresden, Germany, 2006.

[4] R. Preu, D. Biro, J. Rentsch, F. Clement, D. Erath, G. Emanuel, A. Grohe, M. Hofmann, A. Mette, C. Voyer, W. Wolke, S. W. Glunz, and G. P. Willeke, "The status of silicon solar cell production technology development at fraunhofer ise," presented at Proceedings of the 4th World Conference on Photovoltaic Energy Conversion, Waikoloa, Hawaii, USA, 2006.

[5] J. F. Nekarda, L. Gautero, S. Stumpp, A. Grohe, D. Biro, and R. Preu, "LFC on screen printed Aluminium rear side metallization," presented at 24th European Photovoltaic Solar Energy Conference and Exhibition, Hamburg, Germany 2009.

[6] A. Wolf, S. Mack, E. A. Wotke, A. Lemke, C. Bertram, U. Belledin, D. Biro, and R. Preu, "The SiNTO Process: Utilizing a SiNX Anti-Reflection Layer for Emitter Masking During Thermal Oxidation," presented at Proceedings of the 34th IEEE Photovoltaics Specialists Conference (PVSEC), Philadelphia, PA, 2009.

[7] W. Kern and D. Puotinen, "Cleaning solutions based on hydrogen peroxide for use in silicon semiconductor technology," *RCA Review*, vol. 31, pp. 187, 1970.

[8] A. Lemke, H. Furtwängler, J. Rentsch, D. Biro, and R. Preu, "Thermal oxidation and wet chemical cleaning of silicon wafers for industrial solar cell production," presented at Proceedings of the 22nd European Photovoltaic Solar Energy Conference, Milan, Italy, 2007.

[9] J. Seiffe, L. Weiss, M. Hofmann, L. Gautero, and J. Rentsch, "Alternative rear surface passivation for industrial cell production," presented at Proceedings of the 23rd European Photovoltaic Solar Energy Conference, Valencia, Spain, 2008.

[10] E. Schneiderlöchner, A. Grohe, B. Fleischhauer, M. Hofmann, S. W. Glunz , R. Preu, and G. Willeke, "Status and advancement on transferring the laser-fired contact technology to screen-printed silicon solar cells," presented at Proceedings of the 20th European Photovoltaic Solar Energy Conference, Barcelona, Spain, 2005.

[11] M. Hofmann, D. Erath, B. Bitnar, L. Gautero, J. Nekarda, A. Grohe, D. Biro, J. Rentsch, and R. Preu, "Industrial type CZ silicon solar cells with screen-printed fine line front contacts and passivated rear contacted by laser firing," presented at Proceedings of the 23rd European Photovoltaic Solar Energy Conference, Valencia, Spain, 2008.

[12] A. Cuevas and R. A. Sinton, "Prediction of the open-circuit voltage of solar cells from the steady-state photoconductance," *Progress in Photovoltaics: Research and Applications*, vol. 5, pp. 79-90, 1997

[13] T. Roth, J. Hohl-Ebinger, E. Schmich, W. Warta, S. W. Glunz, and R. A. Sinton, "Improving the accuracy of suns-VOC measurements using spectral mismatch correction," presented at Proceedings of the 33rd IEEE Photovoltaic Specialists Conference, San Diego, USA, 2008.

[14] A. S. H. van der Heide, J. H. Bultman, J. Hoornstra, and A. Schönecker, "Contact resistances measured using the corescan: relations with cell processing," presented at Proceedings of the 17th European Photovoltaic Solar Energy Conference, Munich, Germany, 2001.

[15] F. Huster, "Investigation of the alloying process of screen printed aluminium pastes for the BSF formation on silicon solar cells," presented at Proceedings of the 20th European Photovoltaic Solar Energy Conference, Barcelona, Spain, 2005.

[16] L. Gautero, J. Rentsch, L. Weiss, N. Kohn, S. Eigner, M. Zimmer, J. Specht, J. Nekarda, D. Stüwe, M. Retzlaff, D. Biro, J.-M. Sallese, and R. Preu, "Industrial approach for the deposition, through-vias wet opening and firing activation of a backside passivation layer applied on solar cells," presented at Proceedings of the 23rd European Photovoltaic Solar Energy Conference, Valencia, Spain, 2008.

[17] F. E. Ritter and L. J. Schooler, "The learning curve," 2002.

[18] K. A. Munzer, K. Holdermann, and R. E. Schlosser, "Thin Monocrystalline Silicon Solar Cells," *TRANSACTIONS ON ELECTRON DEVICES,*, vol. 46, pp. 2055-2061, 1999.

[19] A. Mette, "New concepts for front side metallization of industrial silicon solar cells," in *Fakultät für Angewandte Wissenschaften*. Freiburg: Universität Freiburg, 2007, pp. 231.