Properties of SiO_2 and Si_3N_4 as gate dielectrics for printed ZnO transistors

S. Walther,[a] S. Polster, and B. Meyer
Chair of Electron Devices, University of Erlangen-Nuremberg, Cauerstrasse 6, 91058 Erlangen, Germany

M. P. M. Jank
Fraunhofer Institute for Integrated Systems and Device Technology, Erlangen, Germany

H. Ryssel and L. Frey
Chair of Electron Devices, University of Erlangen-Nuremberg, Cauerstrasse 6, 91058 Erlangen, Germany and Fraunhofer Institute for Integrated Systems and Device Technology, Schottkystrasse 10, 91058 Erlangen, Germany

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In this article, the authors report on thin film transistors based on gas phase synthesized ZnO nanoparticles using low temperature deposited silicon dioxide and silicon nitride as gate dielectrics. For bottom gate transistors, the devices using silicon nitride as gate insulator show the lowest off-current for a given induced charge and the steepest subthreshold slope. The charge carrier mobility of around 3×10^{-3} $cm^2/V\,s$ and an I_{on}/I_{off} ratio of around 10^5 are almost independent of the insulator material. In a double gated thin film transistor using low stress silicon nitride as a top gate insulator, transistor parameters are extracted for the identical semiconducting layer when the bottom and top gates are used. It is shown that the extracted charge carrier mobility is not inherent for the ZnO nanoparticle layer but rather an effective value for the device under investigation.
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I. INTRODUCTION

In recent years, there has been substantial interest in the realization of large area electronic systems by printing techniques. While by conventional complementary metal-oxide semiconductor processing, highly integrated chips can be fabricated, the maximum chip area is limited, besides other factors, by the wafer size. For applications like displays with a low number of functions per area, printing is expected to allow for continuous material deposition on large area substrates such as glass or even polymer foil. Furthermore, an additive rather than a subtractive material deposition could reduce process complexity and cost. For this technology, utilization of nanosized particle dispersions as functional inks seems promising. A variety of semiconducting materials in the form of nanoparticles has been evaluated, e.g., CdSe (Ref. 1) and PbSe.[2] Among these, ZnO has been found as a nontoxic candidate for the realization of printed *n*-type metal-oxide semiconductor devices. ZnO is a wide band gap semiconductor that shows a high charge carrier mobility when employed as an active layer in transistors fabricated, e.g., by sputtering at room temperature.[3]

In the majority of solution processed ZnO thin film transistors (TFTs) reported in the literature, a wet chemical process is used either to grow particles that are deposited on a substrate[4–8] or to convert a precursor of ZnO to a ZnO film directly on the substrate.[9,10] When particles are grown wet chemically, the process yield is very limited, contamination of the particles with precursor components can occur, and up-scaling is demanding. Conversion of the precursor on the substrate, on the other hand, typically requires relatively high temperatures in the range of 500 °C (Ref. 9) for the reaction, which the substrate has to withstand. Both drawbacks of that route could be overcome by using dispersions of ZnO particles synthesized in the gas phase. The production volume of ZnO particles from the gas phase for other applications is in the range of tons already. A temperature treatment after deposition is only necessary to remove organic components of the dispersion, so the process temperature can be low. The realization of TFTs based on gas phase synthesized ZnO particles has been demonstrated with process temperatures of 300 °C.[11]

Several insulators have been reported in conjunction with devices based on sputter deposited ZnO including silicon dioxide (SiO_2), silicon nitride (Si_3N_4), and aluminum oxide (Al_2O_3).[12–14] The insulator material has been proven to have great influence on transistor performance.

Toward a suitable insulator for printed ZnO transistors, low temperature deposited SiO_2 and Si_3N_4 are investigated as gate dielectrics in terms of resulting transistor performance.

II. EXPERIMENT

We utilized ZnO nanoparticle powder fabricated in the gas phase by Evonik-Degussa GmbH with a primary particle size of 20 nm. As Reindl *et al.*[15] had shown, a grinding step is necessary to obtain stabilized dispersions as the basis of thin and uniform films from a highly agglomerated powder. Therefore, a suspension of ZnO powder in ethanol was dispersed with a Lau disperser DAS H 200-K using yttrium stabilized zirconia milling beads. The dispersion contained 20 wt % ZnO and was stabilized by 3 wt % 2-[2-(2-methoxyethoxy)ethoxy]acetic acid [trioxadecanoic acid (TODA)] with regard to the mass of the ZnO nanoparticles.

[a]Author to whom correspondence should be addressed; electronic mail: sabine.walther@leb.eei.uni-erlangen.de

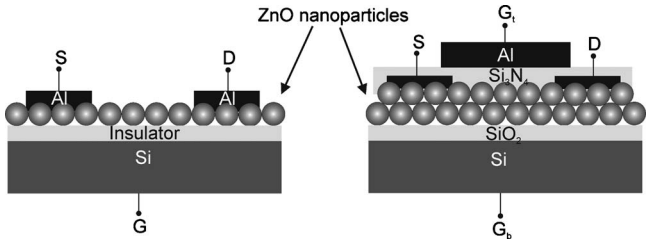


FIG. 1. Schematics of a bottom gate ZnO TFT and a double gate ZnO TFT.

One-third of the volume of the milling vessel (Schott–Duran) was subjected to the milling beads. For 50 ml vessels, 72 g of milling beads was used. Shortly before film deposition, the suspension was centrifuged in a Sigma 3K30 centrifuge at 20 000 rpm for 2 min for the bottom gate TFTs and for 1 min for the double gate TFTs, and the supernate was gathered with a pipette. The particle size distribution was obtained via dynamic light scattering using a Honeywell Microtrac Ultrafine particle analyzer (UPA 150). The samples for particle size analysis were prepared by diluting the dispersion with ethanol according to an optimal loading factor determined by the measurement setup. Thermogravimetric analysis (TGA) was conducted on a TA Instruments Q 50. Samples of 10–25 mg ZnO nanoparticles were heated from 25 to 850 °C under N_2 at a heating rate of 10 K/min.

Highly *p*-doped silicon was used as a bottom gate electrode. On top of the silicon wafers, 200 nm of SiO_2 and Si_3N_4 were deposited by plasma enhanced chemical vapor deposition (PECVD) at 300 °C. In the case of Si_3N_4, alternate deposition at high and low frequencies was used for stress reduction. In addition, one silicon wafer was thermally wet oxidized at 1000 °C to obtain a 200 nm thick high quality insulator for comparison.

The substrates were spin coated with ZnO nanoparticle dispersions at 2000 rpm to obtain film thicknesses of around 50 nm. Heat treatment was applied to the samples for 30 min at a temperature of 400 °C in air. Source and drain top contacts were deposited by evaporation of aluminum through a shadow mask with channel lengths L of 50–150 μm and channel width W of 3 mm for the bottom gate devices and L of 100–200 μm and W of 20 mm for the top and double gate devices, respectively. Schematics of the resulting devices are depicted in Fig. 1.

The morphology of the ZnO nanoparticle thin films was characterized using a JEOL JSM-7500F scanning electron microscope (SEM) with an acceleration voltage of 15 kV using an in-lens detector. Electrical measurements were conducted in nitrogen atmosphere in a glovebox at room temperature using a source meter instrument 2636 from Keithley. From the transfer characteristics, the threshold voltage was extracted by plotting the square root of the drain current versus the gate voltage and extrapolating the linear region of the curve to the *x*-axis. The charge carrier mobility was calculated in the saturation region according to

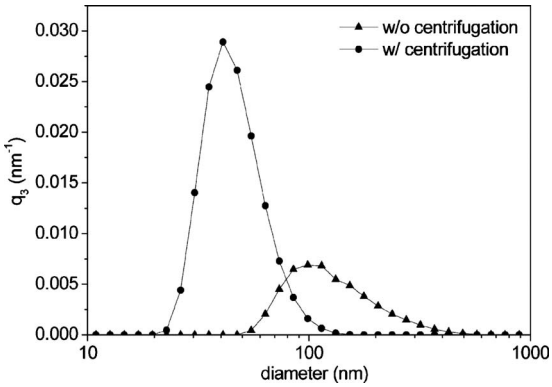


FIG. 2. Volumetric diameter distribution of the dispersion as milled and after centrifugation at 20 000 rpm for 2 min.

$$\mu_{sat} = \left(\frac{\partial \sqrt{I_{DSAT}}}{\partial V_{GS}} \right)^2 \left. \frac{2L}{WC_{is}} \right|_{V_{DS} > (V_{GS} - V_T)}. \quad (1)$$

In this equation, I_{DSAT} denotes the drain current in the saturation region, V_{GS} is the gate voltage, and C_{is} is the capacitance of the insulator. The subthreshold slope was extracted from the maximum value of the derivative of the drain current with respect to the gate voltage.

III. RESULTS AND DISCUSSION

A. Characterization of ink

The ZnO nanoparticle ink was characterized regarding the particle size distribution and the temperature dependent weight loss. In Fig. 2, the volumetric size distribution of the ZnO particles in the as milled dispersion and after centrifugation is shown. In the case of the as milled dispersion, a broad size distribution was found, where the maximum particle size was around 700 nm and the volumetric mean of the diameter was 100 nm. We can conclude that particles are still agglomerated in this case. After centrifugation, however, the size distribution was narrower and shifted to smaller diameters. The maximum size here was around 120 nm; the volu-

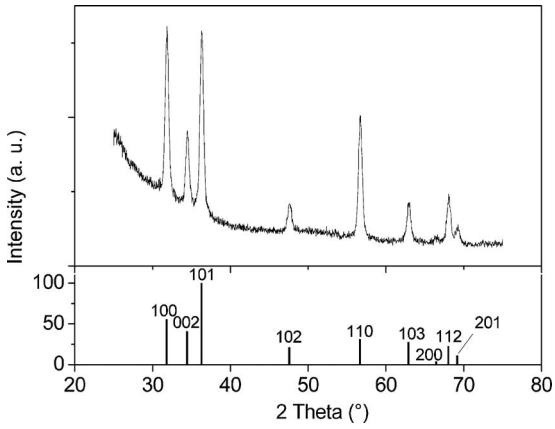


FIG. 3. XRD pattern of a ZnO nanoparticle film deposited from a dispersion centrifuged at 20 000 rpm for 2 min. Also shown is the reference card (PDF 01-070-8070) for ZnO in wurtzite structure.

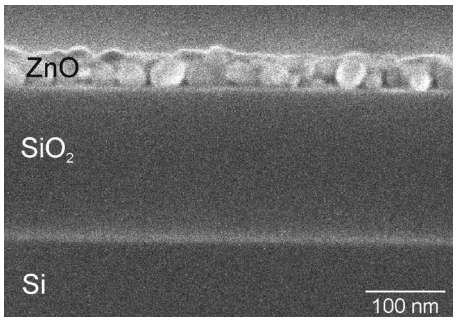


FIG. 4. SEM photograph of a ZnO nanoparticle layer deposited from a dispersion centrifuged at 20 000 rpm for 2 min.

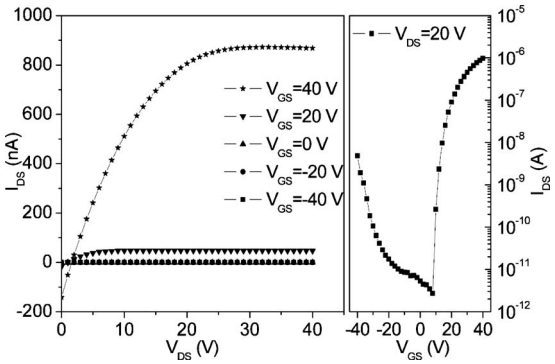


FIG. 5. Output and transfer characteristics of a bottom gate ZnO nanoparticle TFT using thermally grown SiO_2 as gate insulator. The W/L ratio is 60. The negative drain current in the output curves for low drain voltage and the increase in drain current for negative gate voltage in the transfer curve are due to gate leakage current.

metric mean was 40 nm, which corresponds roughly to the primary particle size. The TGA measurement (not shown here) revealed a weight loss starting at around 300 °C and completed at around 400 °C, which indicates the decomposition of the TODA.[8]

B. Characterization of ZnO nanoparticle layer

After film deposition, gracing incidence x-ray diffraction (XRD) measurements were conducted. In Fig. 3, the intensity pattern is shown together with the reference pattern for ZnO in wurtzite structure [pair distribution function, Powder Diffraction File 01-070-8070]. All peaks of the measurement could be related to the reference pattern. No preferred orientation of the crystals on the substrate was observed. A SEM photograph of the cross section of a ZnO nanoparticle film deposited from the dispersion centrifuged for 2 min on a thermally oxidized silicon substrate is shown in Fig. 4. It can be seen that the film is very smooth, and no pinholes were observed. The film thickness was around 50 nm which is very close to the mean diameter of the centrifuged dispersion. In fact, almost a monolayer of ZnO nanoparticles was obtained.

C. Electrical characterization of bottom gate TFTs

In Fig. 5, the output and transfer curves of a typical bottom gate TFT with a gate dielectric of thermally grown SiO_2 are shown. The devices act like *n*-channel enhancement mode transistors showing hard saturation and a quadratic dependence of the drain current on the gate voltage. No significant variation of the curves was observed for repeated testing. For the device depicted in Fig. 5, a charge carrier mobility μ_{sat} of 3.5×10^{-3} $cm^2/V\,s$ was extracted in the saturation regime. An I_{on}/I_{off} ratio of around 10^5, a threshold voltage of 13 V, and a subthreshold slope of 1 V/dec were identified with a W/L ratio of 60. The total number of transistors measured for each variation is shown in Table I along with the mean values and standard deviation for all parameters extracted.

The increase in drain current for high negative gate voltage in the transfer curve and the negative drain current for low drain voltage in the output curves is caused by an unexpectedly high gate leakage current. It should be noted, however, that the ZnO layer covers the whole sample, which makes the sample area of 4 cm^2 the gate area. Nevertheless, the existence of a conduction path between source, drain, and gate along the surface of the ZnO layer over the sample edges cannot be ruled out. Furthermore, the gate leakage current could be enhanced by a modification of the interface between ZnO and SiO_2, leading to, e.g., a lower energetic barrier between ZnO and SiO_2 or to establishment of traps.

TABLE I. Summary of extracted parameters of measured devices.

	Dielectric layer					
	Bottom gate TFTs			Double gate TFTs		
	PECVD SiO_2	PECVD Si_3N_4	Thermal SiO_2	Thermal SiO_2 bottom gate only	PECVD Si_3N_4 top gate only	Double gate
Devices evaluated	10	10	20	3	3	3
μ_{sat} (mean) ($cm^2/V\,s$)	0.0123	0.00455	0.00984	0.00281	0.00561	0.00734
μ_{sat} (standard deviation)	0.0071	0.00245	0.00453	n/a	n/a	n/a
$\log(I_{on}/I_{off})$ (mean)	5.16	5.1	3.83	1.44	1.85	1.93
$\log(I_{on}/I_{off})$ (standard deviation)	0.460	0.568	0.811	n/a	n/a	n/a
V_T (mean) ($cm^2/V\,s$)	10.73	9.89	11.02	6.6	3.175	3.525
V_T (standard deviation)	6.758	1.247	2.100	n/a	n/a	n/a
S (mean) (V/dec)	2.04	0.67	3.76	20.53	8.3	5.8
S (standard deviation)	1.12	0.313	1.46	n/a	n/a	n/a

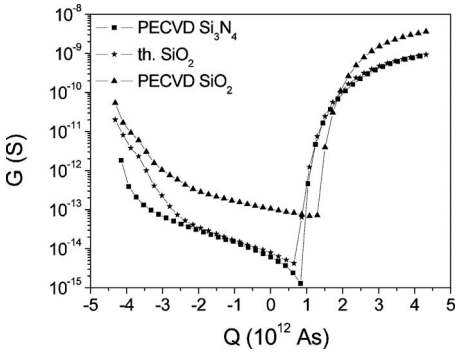


FIG. 6. Transfer characteristics of the bottom gate devices with different gate insulators plotted as conductivity vs induced charge. The W/L ratio is 60 for all devices.

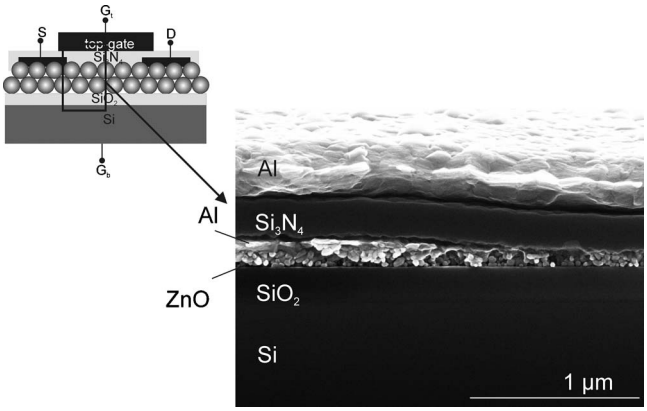


FIG. 7. SEM photograph of the cross section of the double gate ZnO nanoparticle TFT.

The transfer curves measured for transistors using PECVD deposited dielectrics are depicted in Fig. 6. For better comparison, the conductance G calculated from the drain current, the drain voltage, and the W/L ratio (60) is plotted versus the induced charge Q which is a function of gate voltage, dielectric constant of the insulator, and insulator thickness. The transfer curve of the device using PECVD deposited SiO_2 is shifted to higher positive gate voltages with respect to the other devices and reveals an off-current ten times higher than the off-current of the device using thermally grown SiO_2. For the device shown, a saturation mobility of 5.7×10^{-3} $cm^2/V\,s$, an I_{on}/I_{off} ratio of around 10^4, a threshold voltage of 17 V, and a subthreshold slope of 1.3 V/dec were extracted. For the transistor with Si_3N_4 as gate dielectric, a saturation mobility of 2.6×10^{-3} $cm^2/V\,s$, an I_{on}/I_{off} ratio of around 10^5, a threshold voltage of 10 V, and a subthreshold slope of 0.7 V/dec were observed. The extracted values for all devices measured are summarized in Table I. It is noteworthy that the devices using Si_3N_4 as gate dielectric showed the lowest off-current for a given induced charge. From the subthreshold slopes, a maximum interface state density was calculated after Rolland *et al.*,[16] which was in the range of 1×10^{-12} cm^{-2} for all materials.

The extracted parameters of the bottom gate TFTs summarized in Table I show a broad dispersion, which is in the range of the difference of the mean values for the different insulator materials. Unlike in the case of sputtered ZnO devices, no strong dependence of the device performance of the printed ZnO TFTs on the insulator material can be observed. The interface quality between insulator and active film seems to be determined by geometrical rather then material properties. Furthermore, the extracted charge carrier mobility is rather low for all devices, which have been attributed to the small contact area between particles and insulator.[7,11] Consequently, enhancement of the contact between particles and insulator should lead to better apparent charge carrier mobility.

For verification of this assertion, double gated ZnO TFTs with a bottom and a top gate were fabricated where the bottom gate insulator was thermally grown SiO_2 and the top gate insulator was PECVD deposited Si_3N_4. In Fig. 7, a micrograph of the cross section of a resulting device is depicted. The film thickness was 80 nm in this case because the dispersion was centrifuged for only 1 min before deposition. The top insulator conformally covers the surface of the nanoparticle film. Unfortunately, the yield was low for this process. Out of 20 devices, only three fully working TFTs could be achieved. Again, the variation of the results for repeated testing was negligible.

Figures 8(a) and 8(b) show the output and transfer characteristics of the double gate transistor with a W/L ratio of

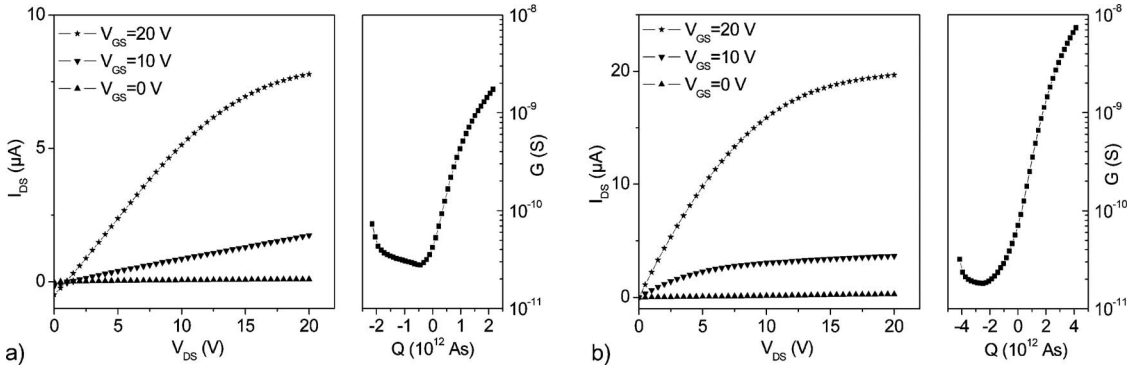


FIG. 8. Output and transfer characteristics of the double gate ZnO nanoparticle TFT controlled by the (a) bottom gate and by the (b) top gate, respectively. The W/L ratio is 200.

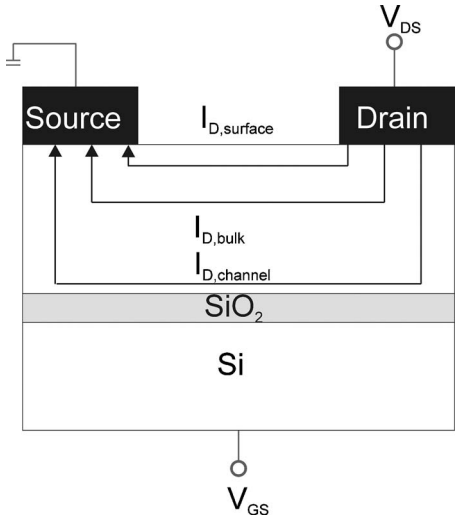


FIG. 9. Schematic of the three-layer model after Wager *et al.* (Ref. 17).

200 when the device was controlled by the [Fig. 8(a)] bottom gate and when the device was controlled by the [Fig. 8(b)] top gate, respectively. In the first case, a saturation mobility of 6×10^{-4} $cm^2/V\,s$, an I_{on}/I_{off} ratio of around 10^2, a threshold voltage of -1.7 V, and a subthreshold slope of 7.8 V/dec were extracted.

The lower I_{on}/I_{off} ratio and the lower subthreshold slope with respect to the bottom gate devices shown in the preceding paragraph can be ascribed to the higher film thickness of the double gate device. According to the three-layer model proposed by Wager *et al.*,[17] three current paths exist in nonoptimized TFTs. As depicted schematically in Fig. 9, current between drain and source can flow through the channel, through the bulk of the active layer, and along the surface. When the channel is turned off, the drain current level is determined by the bulk resistance. For a thicker active layer, the off-current is expected to increase. This was also experimentally confirmed, e.g., by Chung *et al.*[18]

When the top gate was used to control the double gate TFT shown in Fig. 8, a saturation mobility of 4×10^{-3} $cm^2/V\,s$, an I_{on}/I_{off} ratio of around 10^3, a threshold voltage of 2.2 V, and a subthreshold slope of 6.7 V/dec were observed for the identical active channel layer. The charge carrier mobility was nearly ten times higher than the value extracted when the bottom gate was used. The values summarized in Table I for all measured devices give direct evidence for the assumption made above that the extracted charge carrier mobility is an effective value for the device rather than a value inherent for the semiconducting layer. This can be seen from the comparison of the bottom gate devices using SiO_2 and Si_3N_4, respectively, and the double gate device when either the SiO_2 bottom gate stack or the Si_3N_4 top gate stack is used. In the first case, the devices using Si_3N_4 show lower performance; in the latter case, the opposite is the case. It can be concluded that the interface in terms of contact area between the gate insulator and the particle layer is crucial for device performance. This is not the same effect known for classic silicon devices where unsaturated chemical bonds determine the interface quality.

IV. CONCLUSION

In summary, we have fabricated ZnO TFTs with μ_{sat} of $5\times10^{-3}-1\times10^{-2}$ $cm^2/V\,s$, an I_{on}/I_{off} ratio of 10^4 to 10^5 using ZnO nanoparticles synthesized in the gas phase. Our results are comparable to the results of other groups fabricating solution processed ZnO TFTs. Huang and Hsieh[19] reported on ZnO TFTs with an active layer spin coated from a zinc acetate dihydrate solution as a ZnO precursor. At a process temperature of 400 °C, a charge carrier mobility μ_{sat} of 2.35×10^{-2} $cm^2/V\,s$ and an I_{on}/I_{off} ratio of 10^4 to 10^5 were obtained. Furthermore, Adamopoulos *et al.*[20] prepared TFTs with Li doped ZnO active layers fabricated with spray pyrolysis of zinc acetate and lithium acetate dehydrate at 400 °C. A maximum saturation mobility μ_{sat} of 54 $cm^2/V\,s$ and an I_{on}/I_{off} ratio of 10^7 were achieved. However, solution processes using precursor solutions require rather high temperatures for conversion to the desired material. In our approach, the process temperature is determined by the organic additives and can be lowered by an appropriate choice of stabilizers.

ZnO TFTs based on inks containing liquid phase synthesized ZnO nanoparticles were fabricated, e.g., by Faber *et al.*,[7] who obtained a μ_{sat} of 8×10^{-3} $cm^2/V\,s$ and an I_{on}/I_{off} ratio of 10^3 for their bottom gate TFT and μ_{sat} of 2.5 $cm^2/V\,s$ and an I_{on}/I_{off} ratio of 10^6 for their top gate TFT, respectively, at a process temperature of 100 °C.

We have shown that the parameters extracted for our nanoparticle devices are effective values characteristic for the device as a whole. By improvement of the interface between gate insulator and active channel layer, the device performance in terms of apparent charge carrier mobility and I_{on}/I_{off} ratio were enhanced by up to a factor of ten. Conformal deposition of the gate insulator, e.g., by atomic layer deposition, could lead to further improvement of the interface. The authors believe that, with an optimized interface, the performance of ZnO TFTs based on gas phase synthesized nanoparticles would match the performance of TFTs based on liquid phase synthesized ZnO nanoparticles. In summary, utilization of gas phase synthesized nanoparticles promises to be a route to high volume low cost realization of printed electronics.

ACKNOWLEDGMENTS

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[1]B. A. Ridley, B. Nivi, and J. M. Jacobson, Science **286**, 746 (1999).
[2]D. V. Talapin and C. Murray, Science **310**, 86 (2005).
[3]P. F. Carcia, R. S. McLean, M. H. Reilly, and G. Nunes, Jr., Appl. Phys. Lett. **82**, 1117 (2003).
[4]S. K. Volkman, B. A. Mattis, S. E. Molesa, J. B. Lee, A. de la Fuente Vornbrock, T. Bakhishev, and V. Subramanian, Tech. Dig. - Int. Electron Devices Meet. **2004**, 769.
[5]S. Lee, Y. Jeong, S. Jeong, J. Lee, M. Jeon, and J. Moon, Superlattices Microstruct. **44**, 761 (2008).
[6]B. Sun and H. Sirringhaus, Nano Lett. **5**, 2408 (2005).
[7]H. Faber, M. Burkhardt, A. Jedaa, D. Kälblein, H. Klauk, and M. Halik,

Adv. Mater. **21**, 3099 (2009).
[8]K. Okamura, D. Nikolova, N. Mechau, and H. Hahn, Appl. Phys. Lett. **94**, 183503 (2009).
[9]C. S. Li, Y. N. Li, Y. L. Wu, B. S. Ong, and R. O. Loutfy, J. Phys. D **41**, 125102 (2008).
[10]S. T. Meyers, J. T. Anderson, C. M. Hung, J. Thompson, J. F. Wager, and D. A. Keszler, J. Am. Chem. Soc. **130**, 17603 (2008).
[11]S. Walther, S. Schäfer, A. Reindl, M. Jank, H. Thiem, L. Frey, W. Peukert, and H. Ryssel, Microelectron. Eng. **87**, 2312 (2010).
[12]R. L. Hoffman, J. Appl. Phys. **95**, 5813 (2004).
[13]K. Remashan, J. H. Jang, D. K. Hwang, and S. J. Park, Appl. Phys. Lett. **91**, 182101 (2007).
[14]P. F. Carcia, R. S. McLean, and M. H. Reilly, Appl. Phys. Lett. **88**, 123509 (2006).
[15]A. Reindl, M. Mahajeri, J. Hanft, and W. Peukert, Thin Solid Films **517**, 1624 (2009).
[16]A. Rolland, J. Richard, J. P. Kleider, and D. Mencaraglia, J. Electrochem. Soc. **140**, 3679 (1993).
[17]D. Hong, G. Yerubandi, H. Q. Chiang, M. C. Spiegelberg, and J. F. Wager, CRC Crit. Rev. Solid State Mater. Sci. **32**, 111 (2007).
[18]J. H. Chung, J. Y. Lee, H. S. Kim, N. W. Jang, and J. H. Kim, Thin Solid Films **516**, 5597 (2008).
[19]H.-C. Huang and T.-E. Hsieh, Nanotechnology **21**, 295707 (2010).
[20]G. Adamopoulos *et al.*, Adv. Mater. **22**, 4764 (2010).