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A *D*-Band GaN Power Amplifier With 28-dBm P_{sat}, a Power Density of 0.2 W/mm^2, and Loss-Optimized Matching Networks

Thomas Zieciak, Philipp Neininger, Christian Friesicke, *Member, IEEE*, Peter Brückner, and Rüdiger Quay, *Senior Member, IEEE*

***Abstract*—In this letter, we present a *D*-band power amplifier (PA) monolithic microwave integrated circuit (MMIC), manufactured in a gallium nitride (GaN)-on-silicon carbide (SiC) high electron-mobility transistor (HEMT) technology. The PA comprises six stages of 70-nm gate-length HEMTs and features 4-way corporate power combining, which results in an output stage gate-width of 352 μm. We develop and analyze a loss-optimized interstage matching network (ISMN) topology, which is crucial for driving the output stage. As a result, the PA delivers a saturated output power (P_{sat}) of more than 25.2 dBm between 125 and 151 GHz, and a peak P_{sat} of 28 dBm at the center of the frequency band. The high P_{sat} and a small chip size (3.125 mm^2) translate into a power density (P_{dens}) of more than 0.2 W/mm^2. To the best of our knowledge, this PA MMIC demonstrates the highest P_{sat} and P_{dens} beyond 120 GHz across all technologies.**

***Index Terms*—*D*-band, gallium nitride (GaN), high electron-mobility transistor (HEMT), monolithic microwave integrated circuit (MMIC), power amplifier (PA).**

I. Introduction

THE *D*-band, ranging from 110 to 170 GHz, offers high bandwidth and relatively low atmospheric attenuation. Hence, it is considered a promising candidate for next-generation communication systems that target data rates of up to 100 Gbit/s [1]. For a practical link at this frequency, however, the challenge is to realize a transmission range in the order of 100 m. One strategy to achieve this is to increase the EIRP of the transmitter, which either requires a higher PA output power or a higher antenna gain. The latter can be increased by adopting antenna arrays, which require compact active front-ends, thus PAs with high power density (P_{dens}).

There is only a limited selection of monolithic microwave integrated circuit (MMIC) technologies available, providing both high output power and high P_{dens} at *D*-band. Li et al. [2] showcase a Doherty PA with more than 180-mW P_{sat}. The underlying 250-nm SiGe-technology features an advanced back-end-of-line (BEOL), which allows for a small chip size of just 1.1 mm^2 and a high P_{dens} of 0.17 W/mm^2.

Received 14 February 2026; revised 10 March 2026; accepted 21 March 2026. This work was supported by the Federal Ministry of Research, Technology and Space of Germany through Project 6G-TERAKOM under Grant 16KISK158. *(Corresponding author: Thomas Zieciak.)*

The authors are with Fraunhofer Institute for Applied Solid State Physics IAF, 79108 Freiburg im Breisgau, Germany (e-mail: thomas.zieciak@iaf.fraunhofer.de)

This article was presented at the IEEE MTT-S International Microwave Symposium (IMS2026), Boston, MA, USA, June 7–12, 2026.

Digital Object Identifier 10.1109/LMWT.2026.3678195

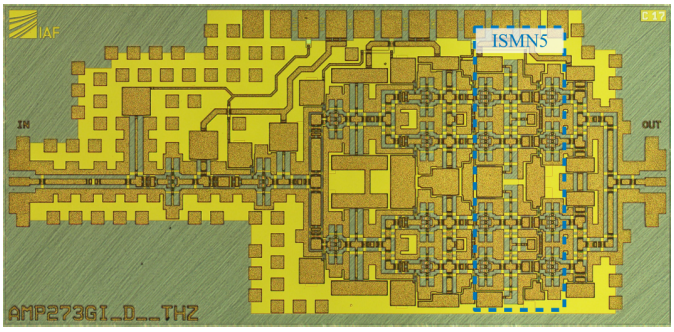

Fig. 1. Micrograph of the PA MMIC with a chip size of 2.50 × 1.25 mm^2.

Alizadeh et al. [3] report on a PA, based on a 250-nm InP-technology, that achieves a peak P_{sat} of 27.4 dBm and a P_{dens} of 0.18 W/mm^2. Finally, there are a number of gallium nitride (GaN)-based publications [4], [5], [6], [7], [8], that all achieve more than 22-dBm P_{sat}. Remarkably, Ćwikliński et al. [4] demonstrate a P_{sat} of 26.4 dBm at 120 GHz by adopting a cascode topology. Due to their relatively simple BEOL, GaN-MMICs are typically more space-consuming. Thus, the presented PA suffers from a low P_{dens} of 0.06 W/mm^2.

The GaN-PA, we present in this letter aims to fill that gap and shall present an attractive candidate for a *D*-band communication system. Correspondingly, it is optimized for high output power and high P_{dens}, hence, small chip size. The target frequency band ranges from 130 to 150 GHz.

This letter structure is as follows. In Section II, we describe the technology and vital design methodologies. Section III reports on various measurement results and Section IV summarizes the results.

II. Technology and Design Methodology

A micrograph of the PA MMIC is displayed in Fig. 1. It is manufactured in Fraunhofer IAF's GaN10-20 technology, which offers a transit (f_{T}) and maximum oscillation frequency (f_{max}) of 145 and 380 GHz, respectively [9]. Fig. 2 shows a simplified schematic of the MMIC. The PA comprises six stages, ensuring sufficient drive for the output stage.

The output stage consists of four 4 × 22 μm high electron-mobility transistors (HEMTs) with source lines, which boost the gain to 6 dB and reduce the gain variation over the target frequency band to less than 1 dB [8]. At *D*-band, the HEMT's

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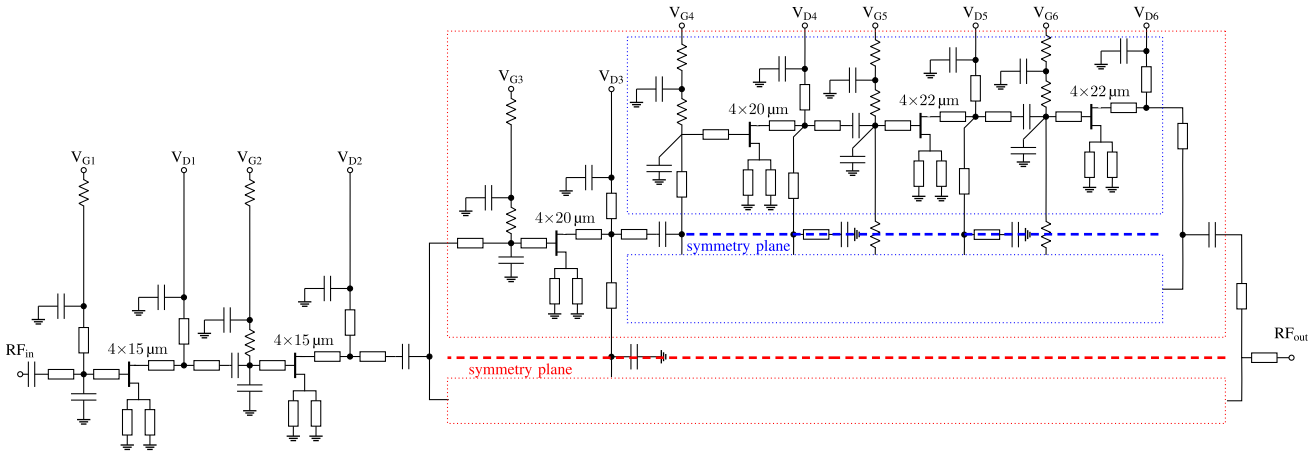

Fig. 2. Simplified schematic of the 6-stage PA MMIC.

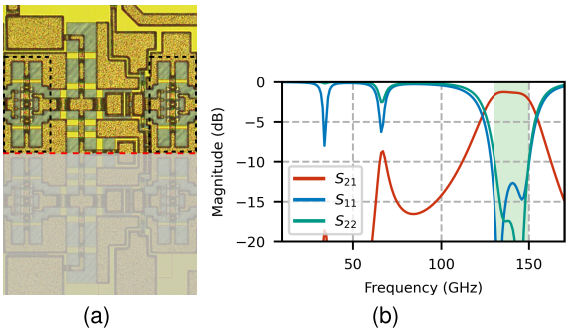

Fig. 3. (a) Breakout section of ISMN5, stage 5 HEMT, and stage 6 HEMT, and (b) EM-simulated and renormalized S-parameters of ISMN5.

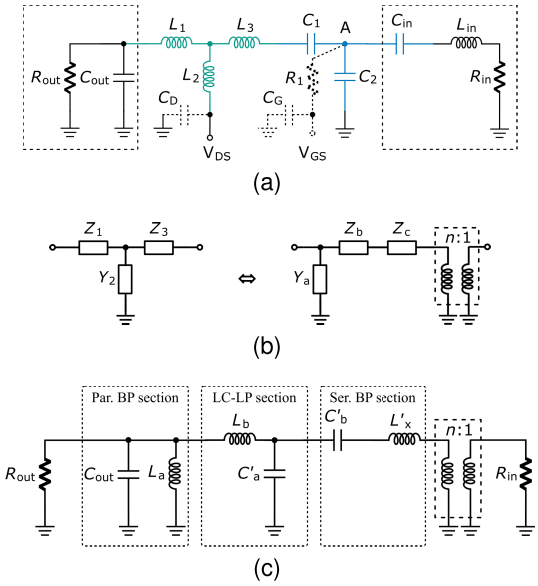

Fig. 4. Simplified schematic of a single branch of ISMN5, the HEMT output port of stage five, and the HEMT input port of stage six (a) before and (c) after application of reverse "TEE"-type partial Norton transformations. Furthermore, (b) reverse "TEE"-type partial Norton transformation identity.

gain rolls off significantly. Under large-signal operation, the device gain compresses even further, making loss optimization of the matching networks the fundamental challenge. Consequently, the output matching network (OMN) is designed as a second-order bandpass. It compensates the HEMT's output

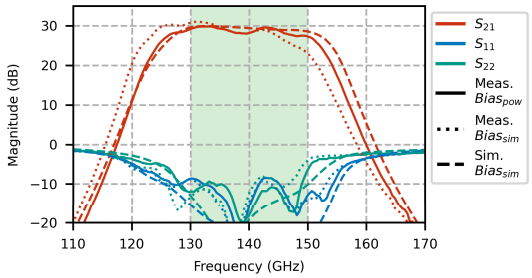

Fig. 5. Simulated (dashed) and measured (dotted) S-parameters of the PA MMIC, biased with Bias_{Sim} as well as with Bias_{Pow} (solid).

capacitance, using inductive stubs and matches to a loadline of $R_{\text{LL}} = 193\ \Omega$. Since the OMN combines four HEMTs in parallel, R_{LL} inherently reduces to 48.25 Ω, which is conveniently close to 50 Ω. As a result, the OMN does not require further impedance transformation, which keeps the network topology simple and therefore favors low insertion loss.

Premature driver-stage compression represents an additional bottleneck. Hence, a conservative gate-width staging-ratio of 1.0 : 1.0 : 2.7 : 5.4 : 5.9 : 5.9 is adopted. For the same reason, minimizing the insertion loss of the interstage matching networks (ISMNs) is critical, too. However, the ISMNs have to match a complex impedance to a complex impedance. This typically requires more network elements, which increases the insertion loss for a given bandwidth and matching target. Therefore, a simple network topology that minimizes the number of required elements but still enables bias insertion and impedance matching must be found.

Fig. 3(a) shows a breakout section of ISMN5. Due to symmetry, the network can be analyzed in isolation from its neighboring branches. The associated simplified schematic is depicted in Fig. 4(a). The elements in the dashed boxes (R_{out}, C_{out} and R_{in}, C_{in}, and L_{in}) represent a fit of the respective HEMT ports, whereas all other components describe the ISMN itself. The drain and gate bias voltages V_{DS} and V_{GS} are supplied via L_2 and R_1, respectively. C_{G} and C_{D} serve as bypassing capacitors. R_1 does not load the low-impedance node A, since it is in the kiloohm range. The dashed components R_1, C_{G}, and C_{D} are solely responsible for biasing. At D-band they can be disregarded, since they either act as open or short circuits. For further analysis, reverse "TEE"-

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TABLE I

SUMMARY OF THE STATE OF THE ART OF GaN PA MMICs AS WELL AS BEST-IN-CLASS SiGe AND InP PA MMICs, OPERATING BEYOND 120 GHz

Ref.	Year	Tech.	l_g(nm)	Freq (GHz)	BW (%)	P_{sat}(dBm)	PAE_{max} (%)	$OP_{1\text{-}dB}$(dBm)	A(mm^2)	P_{dens}($\frac{W}{mm^2}$)
[2]	2022	SiGe HBT	250	107 - 135	23.0	22.7 - 22.4	18.7 - 16.1	18.5 - 14.5	1.11	0.17
[3]	2025	InP HBT	250	126 - 152	18.7	27.4 - 26.0	16.4 - 13.0	27.2$^{\$}$	3.0	0.18
[4]	2019	GaN HEMT	100	107 - 148	32.2	26.4 - 17.0	16.5 - 1.0	25.0 - 14.0	7.5	0.06
[5]	2022	GaN HEMT	40	136 - 136	0	23.5 - 23.5	7.9 - 7.9	19.7 - 19.7	4.25	0.05
[6]	2024	GaN HEMT	100	110 - 170	42.8	22.6 - 15.0	2.8 - 0.1	17.3 - 4.1	5.0	0.04
[7]	2025	GaN HEMT	40	128 - 150	15.8	24†	9†	24†	5.4	0.05
[8]	2025	GaN HEMT	70	129 - 152	16.0	23.2 - 20.6	8.6 - 5.4	18.8 - 16.9	1.6875	0.12
This work	2025	GaN HEMT	70	125 - 151	19.0	28.0 - 25.2	9.0 - 4.7	25.3 - 19.1	3.125	0.2

$^{\$}$ at 150 GHz — † at 145 GHz

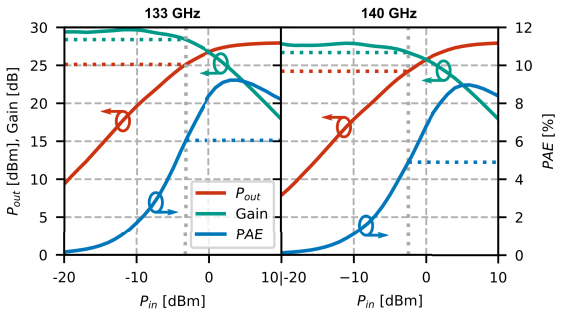

Fig. 6. Measured large-signal parameters of the PA MMIC, biased with Bias_{Pow} versus input power at (left) 133 GHz and (right) 140 GHz.

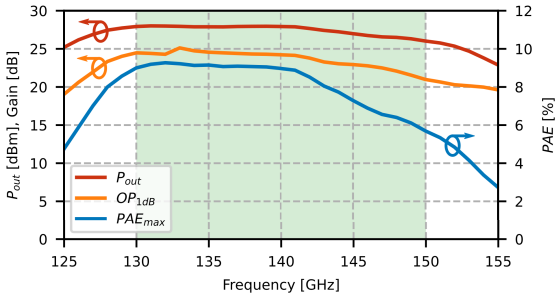

Fig. 7. Measured large-signal performance of the PA MMIC, biased with Bias_{Pow} (V_{DS} = 14 V and j_{DS} = 350 mA/mm) versus frequency.

type partial Norton transformations [10] must be applied. As depicted in Fig. 4(b), they describe a conversion between T- and L-shaped networks with a subsequent ideal transformer. However, there are two important restrictions: first, the T-shaped networks must consist exclusively of either inductors or capacitors, and second, the transformations can only transform impedance downward from left to right. Applying Norton transformations to the green and blue colored subnetworks as well as some rearrangements based on fundamental transformer theory, the schematic can be reorganized as depicted in Fig. 4(c). The transformer ratio n and the element values for L- and C-transformations can be computed according to the following equations:

$$L_a = \frac{L_1}{1-n} \qquad L_b = \frac{L_3}{n^2} + L$$
$$L = \frac{(1-n)\,L_b}{n^2} \qquad n = \frac{1}{1+\frac{L_1}{L_2}} \tag{1}$$

$$C_a = C_2 n \qquad C_b = n\frac{CC_3 n}{C + C_3 n}$$
$$C = \frac{C_2 n}{\left(\frac{1}{n}-1\right)} \qquad n = \frac{1}{1+\frac{C_2}{C_1}}. \tag{2}$$

Compared with a fourth-order bandpass network, which represents the most common ISMN topology, the second and third bandpass sections collapse into a single LC-lowpass section. This cuts the element count by two, yielding a third-order bandpass with lower insertion loss. Fig. 3(b) displays the EM-simulated and renormalized S-parameters of ISMN5. Within the target frequency range, the network achieves excellent impedance matching and an insertion loss between 1.3 and 2.3 dB. Interestingly, the network acts as a quasi-second-order network, since the third pole, which is contributed by the parallel bandpass section, is shifted to 67 GHz. Additional poles below 50 GHz originate from the transparency of C_{D} at low frequencies. They are considered parasitic and, therefore, are ignored for this analysis.

III. MEASUREMENT RESULTS

The S-parameters are acquired by on-wafer measurements, using a PNA-X VNA and VNAX *D*-band frequency extenders. In contrast, the power measurements were carried out on diced samples that were glued to metallic carriers for better heat dissipation. The power-measurement setup supports scalar measurements and includes the following components: an E8257D signal generator, which drives a ×12 frequency multiplier with an integrated preamplifier to produce medium-power *D*-band tones. Next, the signal is passed to a VDI *D*-band power amplifier (PA). Beforehand, it is leveled, using a 3-dB attenuator, to prevent excessive generation of harmonic signal content. Finally, the signal is routed through a motorized attenuator and then fed to the DUT through a probe. On the output side, the signal is picked up with a probe and measured by a PM5 power meter and sensor, which is protected by a high-power 10-dB attenuator. The setup is calibrated by measuring an on-chip THRU calibration standard across the *D*-band in 1-GHz steps. The results are corrected for the 10-dB attenuator and the probe, whose losses were characterized with a VNA beforehand. Unless otherwise noted, all measurements use Bias_{Pow}: V_{DS} = 14 V and j_{DS} = 350 mA/mm.

Fig. 5 shows the S-parameters of the MMIC throughout the full *D*-band. The dashed lines correspond to simulations at V_{DS} = 10 V and j_{DS} = 350 mA/mm (Bias_{Sim}). The dotted and solid lines display measurements using Bias_{Sim} and Bias_{Pow},

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respectively. The measured characteristic is shifted by approximately 5 GHz downward in frequency. However, increasing V_{DS} to 14-V counteracts the shift by slightly decreasing the HEMT's C_{gd} and C_{ds}. Consequently, the 3-dB bandwidth stretches from 125 to 151 GHz, which equates to a 19 % fractional bandwidth. The $|S_{21}|$ is 30 dB at 133 GHz. Moreover, the $|S_{11}|$ and $|S_{22}|$ are below −8 dB between 125 and 155 GHz and below −9 dB between 128 and 149 GHz.

Fig. 6 presents the measured large-signal performance of the PA MMIC under a continuous-wave input power sweep at 133 and 140 GHz. At 140 GHz the PA saturates at an output power of 28 dBm for an input of 10 dBm. The *PAE* reaches its peak value of 9 % at 5-dBm input. Moreover, at an input power of −2.5 dBm, the gain compresses by 1 dB, which is indicated by the gray vertical and teal horizontal dotted lines. Correspondingly, the red horizontal dotted line marks the $OP_{\text{1-dB}}$, which is as high as 24 dBm. The *PAE* at $OP_{\text{1-dB}}$ is 5 % as determined by the blue horizontal dotted line.

Fig. 7 shows the same metrics over frequency. Between 125 and 151 GHz the P_{sat}, $OP_{\text{1-dB}}$ and *PAE* remain between 25.2 and 28.0 dBm, 19.1 and 25.3 dBm, and 4.7% and 9.0%, respectively.

Table I summarizes the state of the art of recently published PA MMICs with operating frequencies higher than 120 GHz. The work presented in this letter demonstrates the highest P_{sat} and P_{dens} across all technologies.

IV. Conclusion

This work presents a 6-stage *D*-band GaN PA MMIC, utilizing 4-way power combining. It is manufactured in a 70-nm GaN HEMT technology, with high f_{T} and f_{max}. The ISMNs are designed in a topology with reduced element-count, minimizing the insertion loss. As a result, the PA delivers a record P_{sat} of 28 dBm. Moreover, its compact layout allows the MMIC to achieve a P_{dens} of 0.2 W/mm^2, which also represents a record.

Acknowledgment

The authors further wish to thank the numerous colleagues of the IAF epitaxy and technology departments for excellent wafer growth and processing.

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