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The Potential of Cast Silicon

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ABSTRACT

The interest in cast mono silicon is increasing due to its lower energy consumption and resulting smaller carbon footprint, lower oxygen content and resulting less oxygen-related defects as well as easy scalability to large wafer formats like 210x210 mm² full square. As a cast silicon alternative to high performance multicrystalline (hpm) silicon, which rapidly lost market share, we analyze the cell efficiency potential of cast mono silicon in a TOPCon cell structure.

We show how the absence of grain boundaries and the exceptional tolerance of the material quality towards high temperature processing enable this significant increase of the cell efficiency potential compared to hpm silicon. The very effective suppression of crystal defects by the Seed Manipulation for ARtificially controlled defect Technique (SMART) results in a very low lateral variation of the high material quality.

We present certified cell efficiencies of 23.3% on n-type material crystallized in our labs, which demonstrates the high efficiency potential even for our lab-type G2 crystallization. An additional crystallization experiment for 210 x 210 mm² wafers demonstrates that SMART mono is compatible to large wafer sizes. A significant difference of the crystallization costs for Cz and cast mono crystallization as a function of electricity costs is discussed.

1. INTRODUCTION

Prices for silicon wafers for solar cells are decreasing steadily e.g. down to values of approx. 0.05 USD/Wp for multicrystalline wafers as reported in the latest ITRPV roadmap [1]. Cast silicon wafers have, in comparison to Czochralski-grown mono silicon a significantly smaller carbon footprint which reflects the lower electricity consumption of this class of material. Cast silicon in this paper refers to all types of silicon which are crystallized in a crucible via the Vertical Gradient Freeze (VGF) technique including traditional multicrystalline, high performance [2], standard cast mono [3], and SMART mono silicon [4].

From the data shown in the ITRPV roadmap from April 2020 [1] it is expected for 2020, that only approx. 7.5 to 9 kWh/kg are needed for the crystallization of cast silicon whereas 30 kWh/kg are consumed to produce Cz silicon. Although the electricity consumption is expected to further decrease slowly in the future a significant gap in energy consumption between both crystallization types will remain according to this study. Please note that in addition to the energy consumption of the crystallization energy is needed for the production of silicon feedstock.

The concentration of interstitial oxygen O_i in cast mono silicon is found to be on the order of 3-5 10^{17} cm^{-3}depending on the applied growth process [5, 6]. This is around a

factor of three lower than in typical Cz-Si materials.

Despite these advantages for cast silicon, the market share of Cz silicon is steadily growing and already exceeded the share of cast silicon in 2019, a trend which is expected to continue in the next years. This observation reflects the difference in technology optimization where Cz silicon production is benefitting from recent developments like multiple ingot pulling by recharging, continuous-feeding or increased growth rate by adapted cooling schemes [7].

Without doubt, the material related cell efficiency potential is a major driving force for the success of a silicon material. It is therefore the aim of this article to demonstrate the efficiency potential of cast silicon and quantify its limitations.

In this paper, we revise different material related limitations of cell efficiency. Based on injection dependent carrier lifetime images of wafers subjected to all cell production relevant temperature processes, we identify and quantify current limits of different types of cast silicon. Comparing new data on cast mono silicon with earlier published data on high performance multicrystalline silicon, we assess the material limits of cast silicon. For this material, we demonstrate the effectiveness of the Seed Manipulation for ARtificially controlled defect Technique (SMART) to avoid crystal defects growing from the crucible edge to the inner part of the ingot. We show how an improved geometry of the monocrystalline silicon seeds and the SMART stacks of functional defects results in a 100% monocrystalline inner silicon ingot.

From our analyses, we predict a high cell efficiency potential for SMART mono silicon material which we have crystallized at Fraunhofer ISE. We tested the robustness of the material at high temperature as they are needed for drive-in emitter processes.

We use for our analysis n-type silicon as it is compatible to our high efficiency TOPCon solar cell process [8]. However, we include in our crystallization experiments also p-type material which is the more common material in industry today.

We confirm our cell efficiency predictions from Efficiency Limiting Bulk Recombination Analyses (ELBA) [9] by TOPCon solar cell processing of 2x2 cm² solar cells reaching efficiencies of up to 23.3%. Recently, the remarkable efficiency potential of cast mono has been confirmed by Canadian Solar who demonstrated a 23.81 % efficient cast mono silicon solar cell of industrial size [10].

2. DEVELOPMENT OF SMART MONO WITHOUT EDGE RELATED STRUCTURAL DEFECTS

The stimulation of monocrystalline crystal growth in cast silicon by using monocrystalline seeds avoids the formation of the typical multicrystalline grain structure occurring in traditional cast silicon processed via VGF crystallization. Structural defects may still occur originating mainly from seed joints, mechanical stress or from the edges of the ingot.

The formation of dislocations at seed joints can be efficiently suppressed by rotating the crystal orientation of one seed plate with respect to the neighboring seed plate while conserving the <100> orientation in growth direction. The rotation can reduce the defected wafer area significantly and thus increases the resultant solar cell efficiency [11].

Mechanical stress may be minimized by optimized temperature fields resulting in a slightly convex crystallization front during growth. Of similar importance is an adapted process with low temperature gradients in the cooling phase in order to minimize long range strain [12].

Structural defects originating from multicrystalline nucleation at the ingot edges may result in inferior crystal quality not only near the edges but also in the center part of the ingot. This effect is visible in Figure 1 on the left: If no further precautions are taken, large angle grain boundaries and especially twin grain boundaries grow diagonally towards the inner filet part of the ingot. In this configuration, grain boundaries and additional dislocations may decrease the crystal quality significantly. The unwanted growth of these defects may be blocked by intentionally introduced functional defects according to the SMART concept [4, 13]. The second column of Figure 1 shows an experimental result from an advanced seed configuration including functional defects. The SMART seed induces the growth of two parallel vertical large angle grain boundaries which restrict the defect growth to its left side. Only at mid-height a grain boundary found its way through the barrier and intrudes into the filet part of the ingot. A 3D reconstruction of a grain boundary, shown as an insert in Figure 1, reveals details of the principal interaction with the SMART boundary. The growth direction is effectively modified to a more vertical growth by the first functional grain boundary plane and can be effectively stopped by the second functional grain boundary plane.

A modified SMART approach for a laboratory crystal growth process for G2 size ingot, shown in the right column of Figure 1, is able to completely contain the defective part of the ingot to the left side of the functional defects which results in a monocrystalline filet part of very high electrical quality. In this configuration, an additional mono seed separates the edge from the SMART stack as a spacer. Most of the parasitic grains nucleated at the crucible were directed back to the ingot edge due to a convex phase boundary near the crucible. Only twin grains were able to overgrow the monocrystalline spacer region. These grains were effectively blocked by the functional defects. The resulting low carrier recombination rates are demonstrated by photoluminescence imaging measurements acquired by the modulum technique [14, 15] (see bottom row of Figure 1). The left measurement demonstrates structural defect induced decreased material quality where the right image reveals the very high electrical quality of the center part of the ingot.

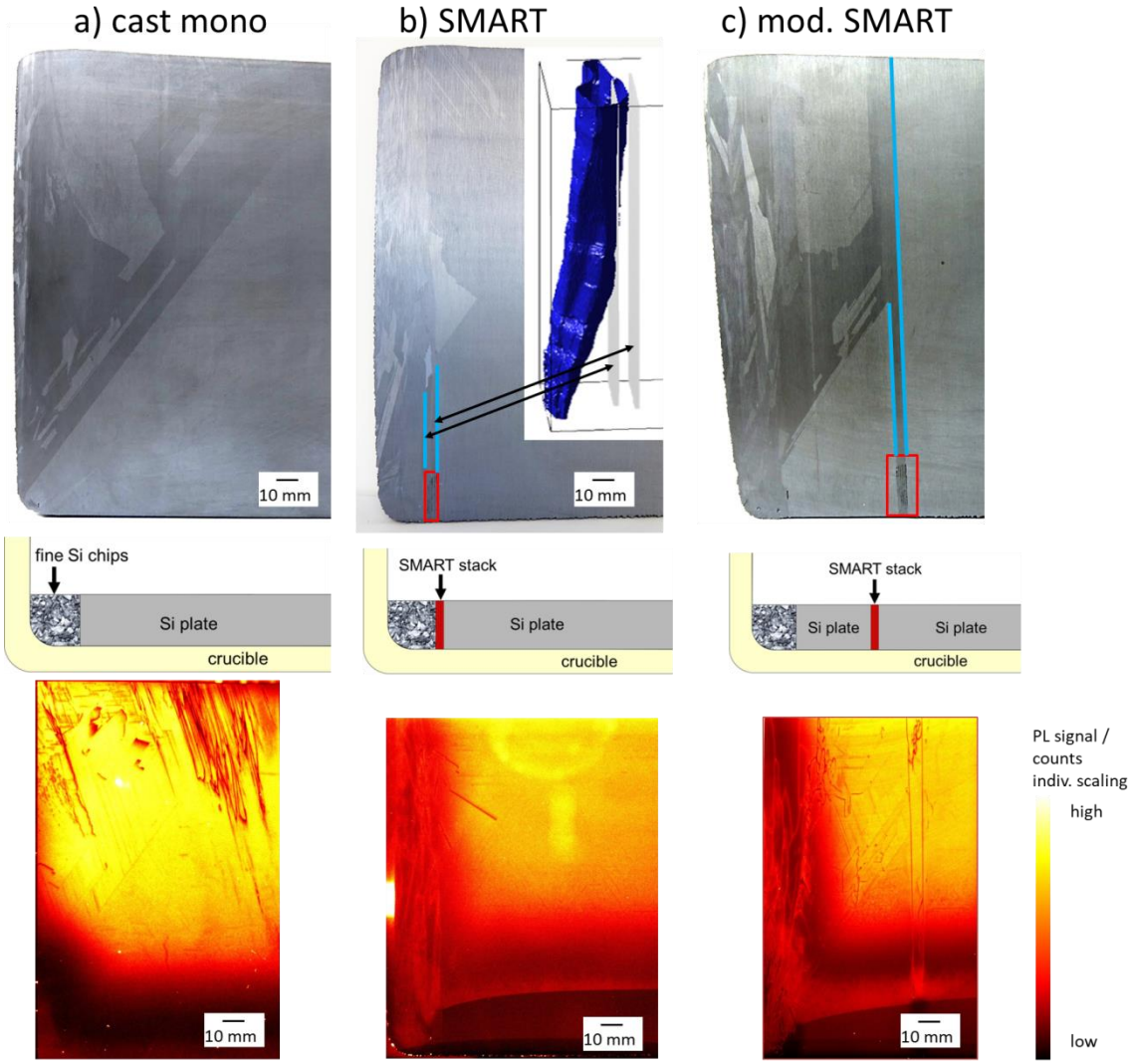


Figure 1. Comparison of cast mono seed concepts: conventional cast mono, SMART and modified SMART approach (from left to right). Top row: Photographs of vertical cuts through the left parts of silicon ingots. Bottom row: Corresponding photoluminescence images revealing recombination centers. The insert in the second image of the top row shows a 3D reconstruction of the grain structure and its interaction with the SMART functional grain boundaries.

The carrier lifetimes of this material with a resistivity of 1.4-1.2 Ω cm on wafer level reached up to 1.5 ms at an injection level of $\Delta n = 10^{15} cm^{-3}$ after a Phosphorous diffusion process.

3. EFFICIENCY POTENTIAL OF MULTICRYSTALLINE AND SMART MONO SILICON

In an earlier study [16] we analyzed the efficiency limits of a TOPCon-based solar cell using high performance multicrystalline silicon. Cell efficiencies of 22.3% have been demonstrated. A loss analysis revealed the most relevant electrical losses to be carrier recombination at grain boundaries and within the emitter.

A consequent step for further optimization of this cell potential is the application of grain-boundary free cast silicon as cast mono silicon. We therefore analyzed the grain-boundary free SMART mono silicon material described in chapter 2 for its general applicability to high efficiency cell processing. We applied a crystallization using a SMART seeding configuration with a targeted resistivity of 0.9 to 0.5 Ω cm as we expected the optimum cell efficiency in this parameter interval from earlier analyses of hpm silicon [17].

In a first test we subjected the wafers to high-temperature processes which are also used in the solar cell processing, i.e. boron diffusion and annealing of the TOPCon layer:

After removing the saw damage (cp etch) and cleaning (RCA) the lifetime samples received a tube furnace boron diffusion at 875°C with one side of the wafer being masked by a PECVD SiOx. Then the boron silicate glass and the SiO_x mask were removed in HF and the wafers were subjected to an oxidation process at 900°C. After removing the thermal oxide, a POCl3 gettering step at 800°C was performed with the boron diffused side also masked by a PECVD SiOx. As a last step the in-diffusions were removed in a wet-chemical process and the wafers were passivated by SiNx.

The wafers' efficiency potential was quantified by Efficiency Limiting Bulk Recombination Analysis (ELBA) [9, 18] based on injection dependent carrier lifetime image stacks from 0.001 suns up to 2.5 suns (we define 1 sun as a photon flux density of $2.5x10^{17}cm^{-2}s^{-1}$ at a wavelength of 808 nm) [19] and a TOPCon cell concept [8], adapted to our case of cast silicon with an efficiency limit of 23.7-23.8% at the investigated resistivity range between 0.5-0.9 Ωcm. For the calculation of this limit for the cell with 875°C boron diffusion and 900°C oxidation step, only Auger recombination has been assumed for carrier recombination in the bulk. Further parameters used are J_{0e} = 30 fA/cm², J_{0rear} = 7fA/cm², R_s = 0.25 Ωcm² and the measured reflectance on reference samples with random pyramids.

For each pixel the measured injection dependent carrier lifetime is used as an input in a numerical cell simulation with Quokka 3 [20].

The resulting cell parameter maps for open-ciruit voltage V_{oc}, fill-factor *FF*, short-circuit current J_{sc} and efficiency η of one example are displayed in Figure 2 together with their respective global values and a comparison with similar data from an hpm silicon wafer [17] with very similar processing temperatures. The hpm silicon ELBA results have been confirmed by solar cells with certified efficiencies of up to 22.3% [16].

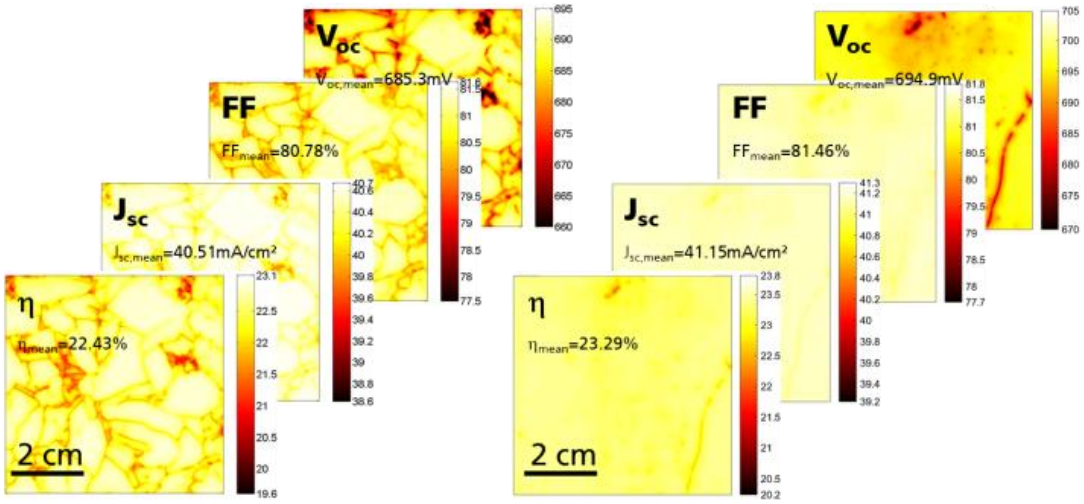


Figure 2. Comparison of ELBA cell efficiency potential analyses of two silicon materials. Left: hpm silicon with a resistivity of 0.75 Ω cm (see [17] for details). Right: SMART silicon with a resistivity of 0.87 Ω cm.

From the ELBA results on the SMART material (J_{0e} = 15 fA/cm^2, high efficiency emitter with an oxidation step at 1050°C) an efficiency gain of approx. 1% absolute can be expected. This calculation assumes a comparable resulting carrier lifetime for both, processing at 900°C and at 1050°C as it is based on carrier lifetime results on wafers processed with slightly lower temperature of 900°C. We further assume that an additional TOPCon-related impact on carrier lifetime by external gettering and possible bulk defect passivation is negligible. We analyzed a variation of base resistivity and included samples with resistivities of 0.55 and 0.87 Ω cm. The carrier lifetime values at maximum power point of the solar cell were 0.78 ms and 1.14 ms, respectively.

It turns out from the results shown in Figure 3 that despite of the higher carrier lifetime and the theoretically slightly higher cell efficiency potential for a material with ideal quality (red dashes) we expect the same resulting cell efficiency for both resistivities.

From this result we can conclude that a crystallization process with resulting resistivities from 1 to 0.5 Ω cm is near the optimum value and will result in cell efficiencies with small variation. This observation is in line with the results on optimum doping concentration for this combination of solar cell process and material quality for hpm silicon. A detailed discussion can be found in [17].

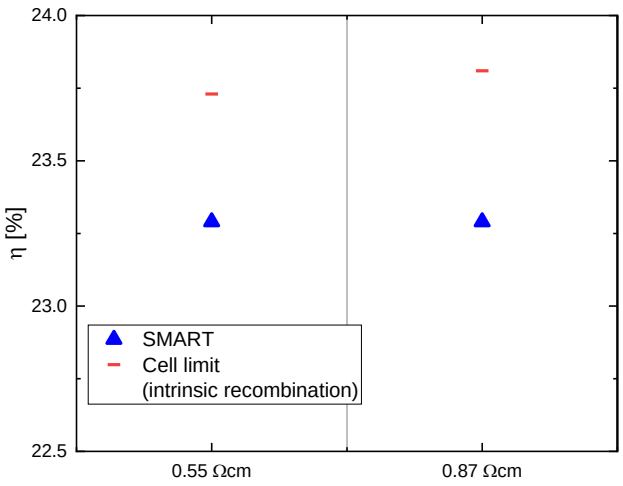


Figure 3. Comparison of theoretical cell efficiencies and ELBA cell efficiency potential analyses for samples with different resistivities. The cell limit assuming only intrinsic recombination in the bulk is shown as red dashes, the ELBA result from carrier lifetime measurements on processed wafers is shown as blue triangles.

As a result of these ELBA analyses we expect the modified SMART material to be a promising choice for high efficient TOPCon solar cell processing on cast silicon. Temperatures of up to 900°C did not degrade the material quality. In the following we show by the presented cell efficiencies that even higher temperatures of up to 1050°C as applied in the cell process are compatible with this material.

4. SOLAR CELL PROCESSING

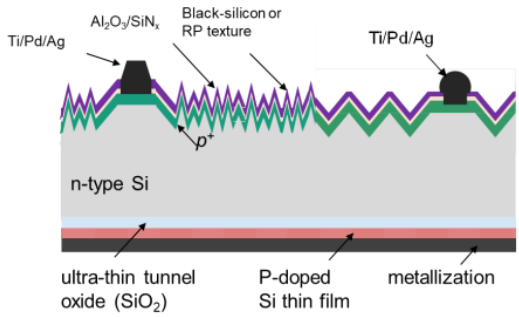
To investigate the *n*-type cast mono silicon at the device level, high-efficiency solar cells with passivating rear side contacts have been processed on *n*-type SMART mono silicon (~200 µm, 0.5-0.9 Ω cm) fabricated at Fraunhofer ISE. For a direct comparison also some wafers of hpm silicon (same material as shown in Figure 2) have been included to the cell processing.

As the first step in the processing of these n-type TOPCon solar cells the active cell area was defined (7 solar cells on each wafer, cell size 20×20 mm^2) and the surface was locally textured. The front side black silicon texture applied for the hpm as well as a part of the cast mono solar cells was realized by a plasma etching step (inductively coupled plasma ICP [21]). The other cast mono solar cells were textured in a standard KOH based solution resulting in a random pyramids surface. To define the active cell area on every wafer, emitter windows were opened in an oxide mask (PECVD SiO_x) and an uniform boron emitter was realized by BBr_3 tube furnace diffusion at 890°C. After an oxide etch (50% HF) the wafers received a drive-in oxidation at 1050°C. After removal of the drive-in oxide the front side was masked by a PECVD SiO_x and a $POCl_3$ diffusion at 800°C was performed. After removal of the PSG the rear side phosphorus doped area was etched by a plasma etching step and then the passivating rear side contact (TOPCon) was deposited and activated by an annealing step at 800°C. As the next step the front side was passivated

by an Al_2O_3/SiN_x layer stack deposited via PA-ALD and PECVD, respectively. The front side contacts were realized by photolithography and evaporation of a Ti/Pd/Ag layer stack. To enhance the electrical contact and completely activate the passivation of front and rear side, the samples received an annealing step in atomic hydrogen (remote plasma hydrogen passivation, 425°C). For the rear side contact, a 1 µm thick Ag layer was evaporated.

For the hpm silicon the processing was restricted to black silicon due to the laterally varying crystal orientation which is not well compatible with an alkaline etching as used for the random pyramids texture.

21 cells have been processed on three parallel wafers near to the position of the 0.87 Ωcm carrier lifetime sample with inhouse efficiencies before double anti reflection coating of 22.7 ± 0.35%. 14 more cells have been processed on two wafers near to the position of the 0.55 Ωcm sample with efficiencies of 22.82 ± 0.16%. The results listed in Figure 4 show that even for this cell process without selective emitter cell efficiencies of up to 23.3% (on 0.9-1 Ωcm SMART mono silicon featuring random pyramids with double antireflection coating) were achieved. Furthermore, the result reveals a remarkably stable material quality even after the applied high temperature step of 1050 °C. This observation is in contrast to the cell results of the hpm silicon cells which only show an efficiency of up to 21.5%. The difference to the best cell efficiency of 22.3% on this material [16] with lower processing temperatures (up to 900°C) can be explained by a respective material deterioration.



Si	Texture	V_{oc} (mV)	J_{sc} (mA/cm²)	FF (%)	η (%)
HPM	b-Si	664.3	40.2	80.5	21.5
SMART	b-Si	689.1	41.2	81.0	**23.0***
SMART	RP	699.0	40.9	81.5	**23.3***

*20x20 mm² Fraunhofer ISE CalLab

Figure 4. Left: TOPCon cell structure which has been used for the cell processing. The surface has been textured either applying a black silicon process or an alkaline etch resulting in random pyramids. Right: Solar cell results on hpm and SMART silicon wafers.

Applying an advanced cell process including a selective front side emitter as described in detail in [22], we may expect even higher efficiency values, if we assume that the carrier lifetime remains stable also for this process (not yet experimentally confirmed). For the measured carrier lifetime in our samples (780 µs for the sample with a resistivity of 0.55 Ωcm and 1.14 ms for the sample with 0.87 Ωcm) Quokka simulations reveal a cell efficiency potential of ~24.5% for both materials.

5. FUTURE OF CAST SILICON

The current market trend as predicted in the ITRPV roadmap [1] is pointing towards a further increase in market share for monocrystalline Cz silicon. Technical progresses like recharging or increased growth velocity have led to a better market position. These steps of technical optimization are still lacking behind in cast silicon. The introduction of a

continuous feeding technique, higher growth rates by advanced cooling schemes and further yield optimization may be part of this optimization. By development of these technological advancements as already implemented in Cz crystal growth techniques a level playing field would be reached in terms of process maturity. This could have a significant impact on throughput and thus cost reduction for the casting processes.

Furthermore, cast silicon has, besides the lower oxygen concentration, two main advantages which are the significantly lower energy consumption and a straight forward adaption of wafer size. In Figure 5 we calculated the total cost of ownership wafer price as a function of the electricity price. Two main messages can be deduced from this result:

(i) Increasing electricity costs favor cast silicon due to their lower electricity consumption per kg silicon. (ii) For M4 wafer size the break-even is expected to be at 3 to 4 cts/kWh, which is decreasing to even lower values for larger wafers of M6 size.

CO_2-pricing would affect the silicon wafer production to a lesser extent for the case of cast silicon compared to Cz silicon.

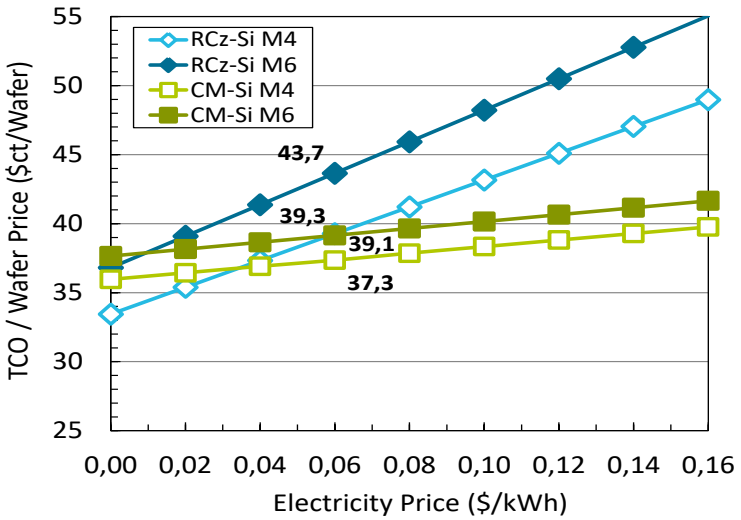


Figure 5. Total cost of ownership calculation of wafer prices as a function of electricity prices for both, Cz and cast mono silicon and for two different wafer sizes M4 and M6.

An experimental confirmation that cast mono M12 crystallization is feasible is shown in Figure 6. In one of our recent p-type crystallization results for the laboratory ingot size G2 equivalent to 75 kg of silicon, we demonstrate the straight forward processing of 210 x 210 mm² (M12) large bricks from the ingot center. In this lab experiment, a monocrystalline crystal growth with high quality over the entire ingot height and cross section large enough for M12 wafers has been realized. The resistivity map acquired by the eddy current method demonstrates a resistivity profile between 1.1 and 0.6 Ωcm with a flat till slightly convex phase boundary. The map of the effective carrier lifetime, which was measured by µPCD, reveals the excellent electrical material quality for the entire center brick with virtually no parasitic grains or dislocation related limitation.

In future work we will produce wafers from this material to verify the excellent material quality with barely any limitations by structural defects as seen on the column sides, which has not been shown yet on this large wafer format M12.

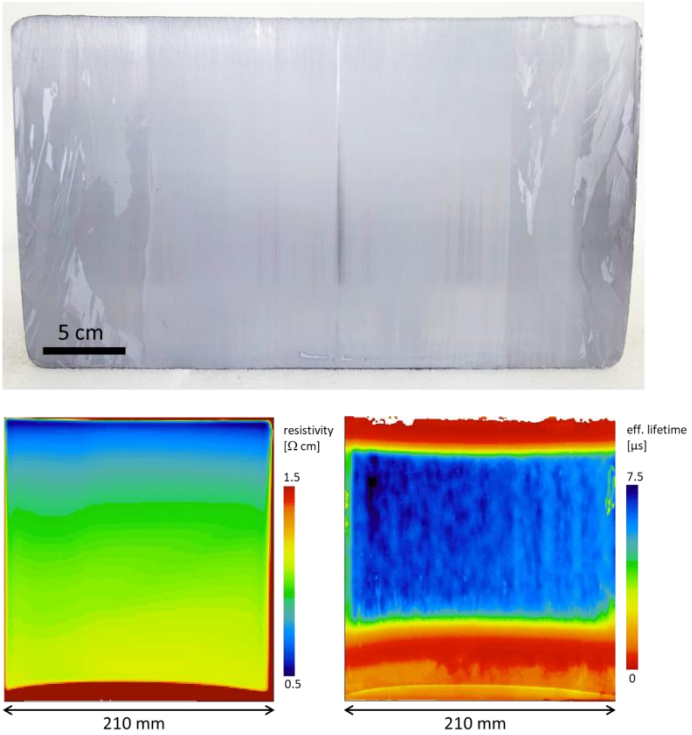


Figure 6. Cross section of a G2 SMART mono ingot with a filet part for a 210 x 210 mm² brick (top) and resitivity (lower left) and effective lifetime measurements (lower right).

6. CONCLUSION

We demonstrated on G2 scale how to crystallize monocrystalline silicon based on a cast mono process with functional grain boundaries. Depending on the used seed configuration in this SMART crystallization concept, structural defects originating from the crucible-silicon interface at the edges could be completely suppressed from bottom to the top of the ingot. This material has been evaluated by ELBA efficiency potential analyses where efficiencies in the range of 23.3% have been predicted for a TOPCon cell process.

Solar cells have been processed and efficiencies of again up to 23.3% have been realized. This result underlines the high efficiency potential of this type of material even for lab-scale ingot sizes and is in line with even higher reported efficiencies of an industrial cell processing on material from larger crucibles with lower impact of crucible related effects.

For both results, ELBA modelling and cell processing we applied a homogeneous emitter without a selective emitter structure in order to reduce the process complexity. A selective emitter could further increase the efficiency potential by combining low recombination and low contact resistance. The presented results show a high temperature tolerance of the modified SMART material up to 1050°C such that selective emitter processes involving such temperatures should be compatible with this material.

Together with the reported transfer to a modified SMART M12 crystallization yielding an excellent material quality also on p-type silicon, we conclude that modified SMART may be, from a scientific point of view, a competitive low-oxygen crystallization option. Our cost calculation show a clear dependence of the wafer prices on both, electricity costs

and wafer size. From these calculation, SMART could be the better option for larger wafers and higher electricity prices for future cell and module concepts.

7. ACKNOWLEDGEMENTS

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