
Parylene Coatings in Power Electronic Modules

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Background, Objective and Method

- **Background:** Double sided cooling (DSC) of power electronic modules → higher power densities and lower parasitic effects. Insulation material with good gap filling capabilities is needed → Parylene coating is highly promising
- **Objective:** Study of parylene F-VT4 and F-AF4 coatings concerning suitability as insulation material in DSC power electronic modules
- **Method:** Assessment of suitability due to individual examination of most important properties:
 - Gap filling capability
 - Adhesion
 - Electrical Insulation
 - Resistance against environmental influences: e.g temperature shock testing

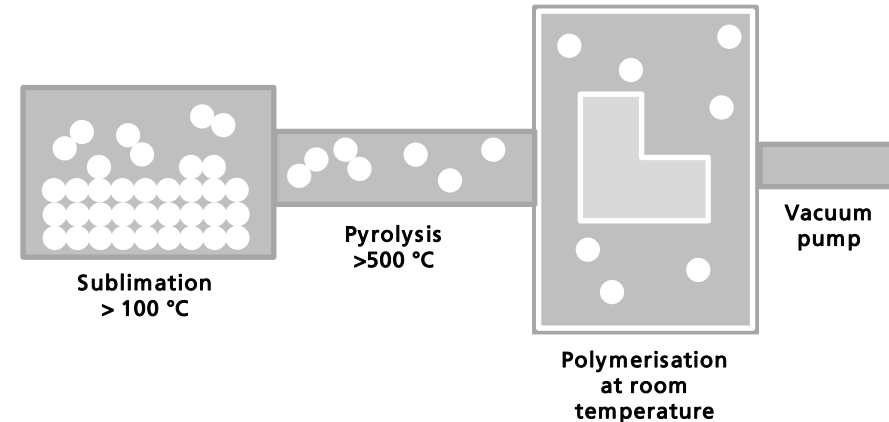
Agenda

- Parylene (poly-p-xylylene) - coating procedure and chosen materials
- Experiments:
 - Gap filling capability
 - Adhesion of parylene coatings
 - Cross-cut testing
 - Pull shear testing
 - Electrical insulation, partial discharge measurements
- Results:
 - Gap filling capability
 - Adhesion of parylene coatings
 - Cross-cut testing
 - Pull shear testing
 - Electrical insulation, partial discharge measurements
- Summary and outlook

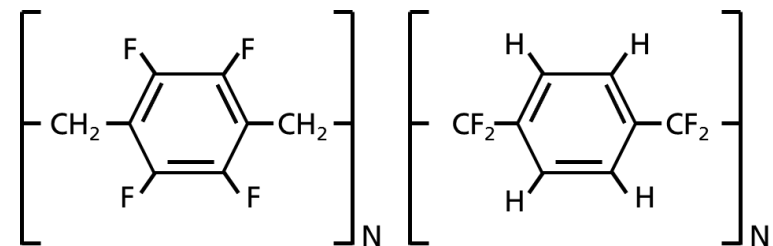
Parylene (Poly-p-xylylene)

Coating Procedure and chosen Materials

- Parylene: group of film forming thermoplastics
- Coating procedure (right top): chemical vapour deposition, steps:
 - 1) Sublimation: parylene dimer powder is heated from solid to gaseous state
 - 2) Pyrolysis: splitting of gaseous dimers to reactive monomers
 - 3) Deposition on the samples and polymerisation



Parylene coating procedure, following [2]



Structural Formula of parylene F-VT4 (left) and F-AF4 (right). Following [3]

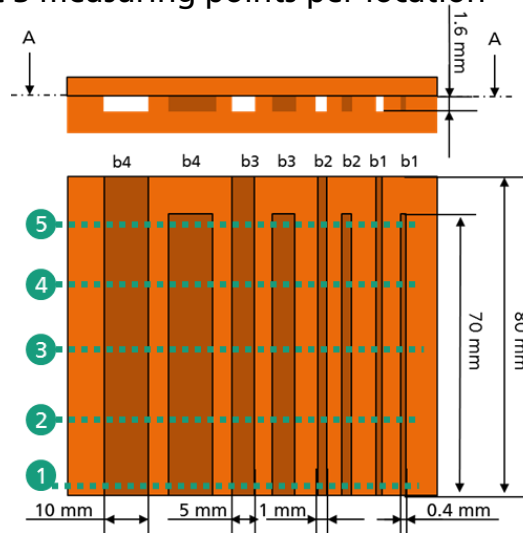
Material Properties	F-VT4	F-AF4
Temporary peak temperature in °C	300	450
Continuous temperature in °C	190	350
Tensile strength in MPa	52	52
Dielectric strength, short time in Volts/mil at 1 mil	5500	5500

Source: PPS: Parylene Properties [1]

Experiment: Gap Filling Capability

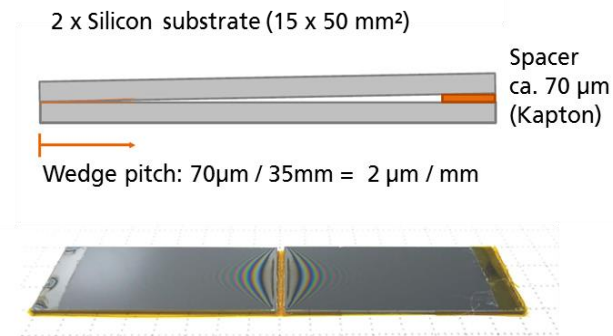
Copper Gap and Silicon Wedge Samples

- Copper sample with differently sized gaps to test the gap filling capability.
- Analysis of the coating thickness in the gaps with reflectometer measurements
- Measurement at 5 different depths. marked by the green dotted lines in each column (a-h) there at least 3 measuring points per location



Sketch of Copper Gap Sample

- Silicon wedge samples with opening of max. 70 μm
- Analysis of the coating thickness with reflectometer measurements
- Analytical examination of the coating thickness distribution with the interference rings

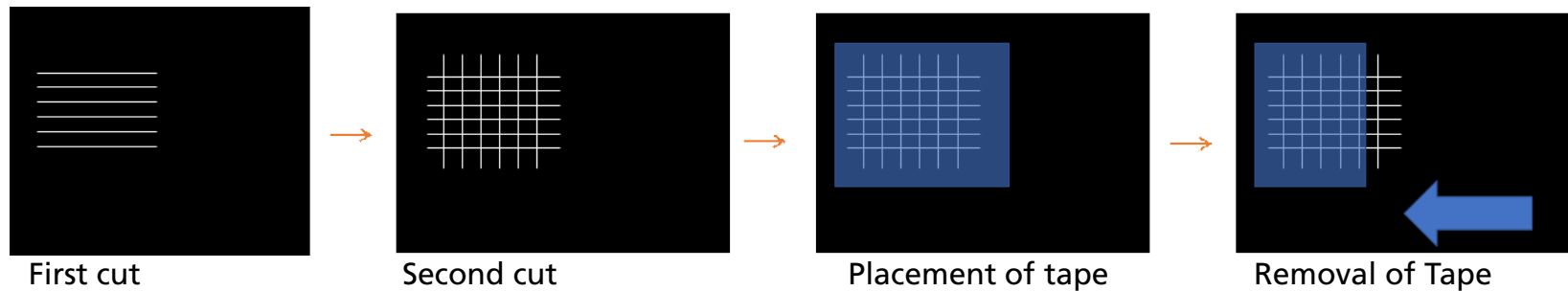


Silicon wedge specimen; sketch from the side (top) and unfolded sample (bottom)

Experiment: Adhesion of Parylene Coating

Cross-cut Testing Test Procedure

Test procedure:



Norms: ASTM D3359, DIN EN ISO-2409-2013

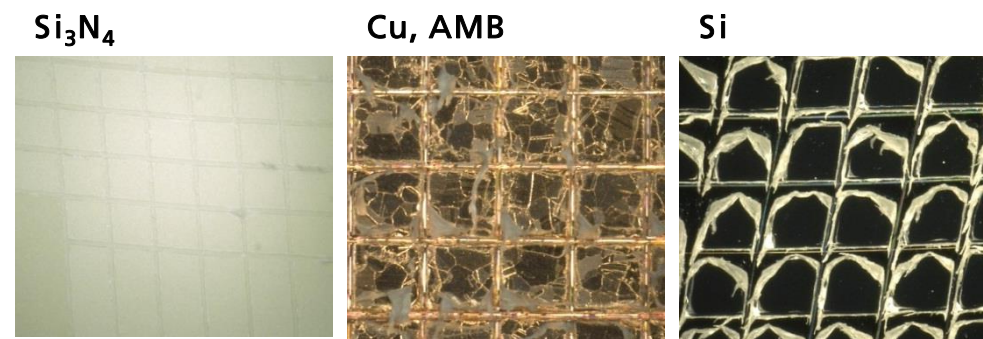
Classification of adhesion test results with percentage of removed area:

Percent Area Removed		0%	Less than 5%	5-15%	15-35%	35-65%	More than 65%
Appearance							--
Classification	ASTM	5B	4B	3B	2B	1B	0B
	DIN	0	1	2	3	4	5

Experiment: Adhesion of Parylene Coating

Cross-cut Testing - Specimens

- Different surfaces:
 - Si_3N_4 ceramics master cards
 - Copper, active metal brazed substrate (AMB) master cards
 - Silicon wafers
- Different types of parylene: F-AF4, F-VT4
- Different cleaning methods: cleaner 1, cleaner 2, reference sample

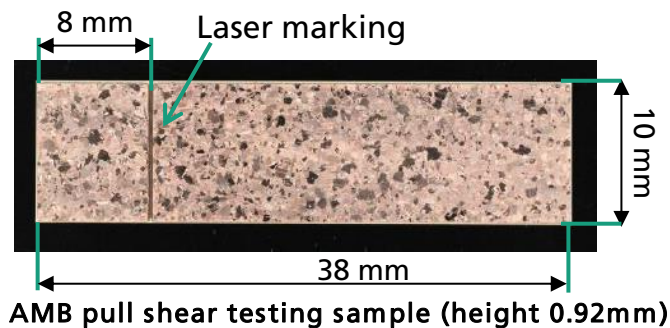


Cross-cuts on different specimens

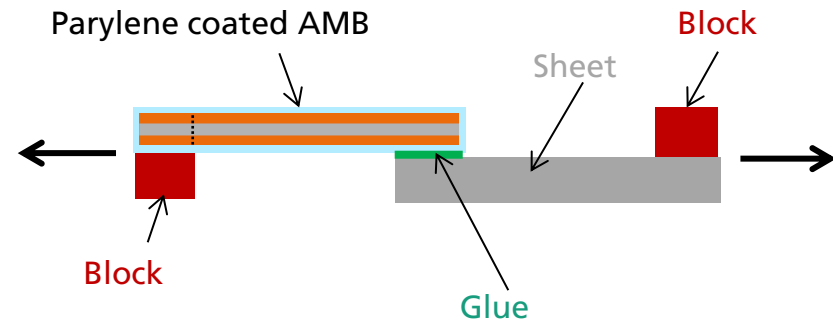
Experiment: Adhesion of Parylene Coating

Pull Shear Testing

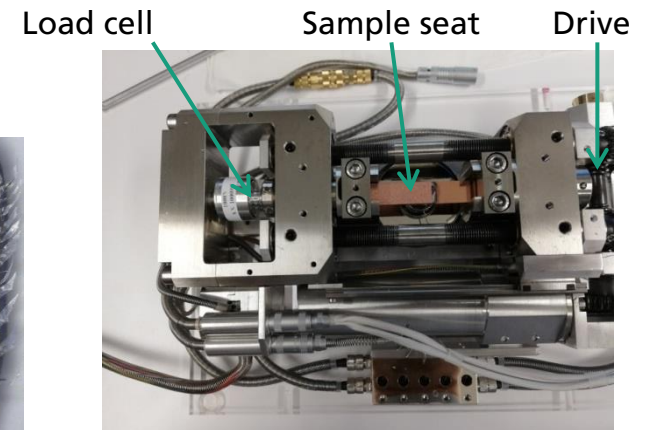
- Pull shear testing of parylene F-VT4 and F-AF4 coated AMB test structures was done before and after temperature shock testing
- AMB samples were glued together with sheets and tested in a pull shear tester
- Before glueing: plasmaactivation
- Glueing was done with a stencil printing tool. glue area was 10 mm x 10 mm, height 80 µm
- Glue: Araldite 2029-1



Parylene on glue



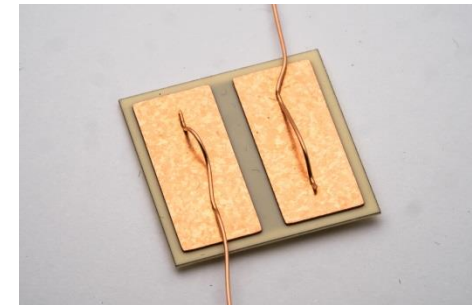
Pull shear testing schematic



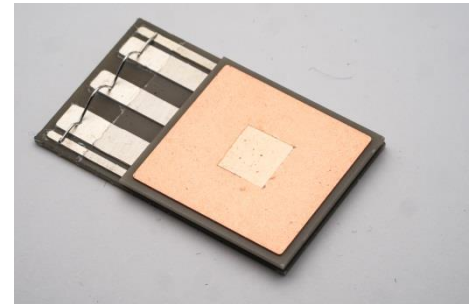
Sample in pull shear tester

Experiment: Electrical Insulation Partial Discharge Measurements

- Ceramic circuit carrier test structures with one insulation gap used for partial discharge measurements before and after temperature shock testing (right side, top)
- In addition partial discharge testing on DSC example substrate (right side, bottom)
- **Partial discharge measurements parameters:**
 - Discharge threshold: 10 pC, according to IEC 61287
 - Frequency: 1 MHz, mains frequency: 50 Hz
 - Velocity: 50 V/s
- **Temperature shock testing parameters:**
 - T_{\min} : -40°C
 - T_{\max} : 220°C
 - 15 min T_{\min} , 15 min T_{\max} (15 min starting from the time the samples have the the min/max temperature) → 30 min T_{\min} , 30 min T_{\max}
 - Tests at 100, 200 and 300 cycles

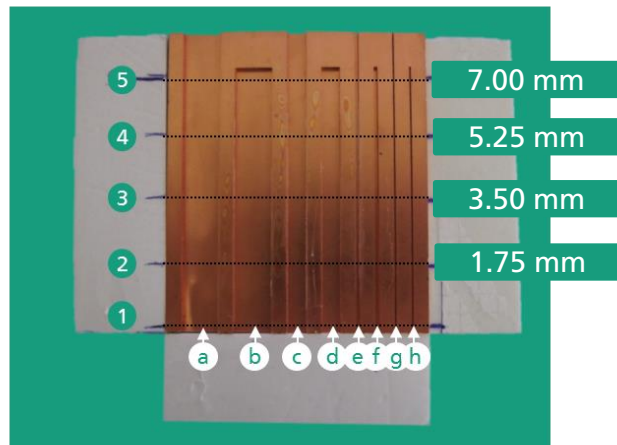


AMB test structure

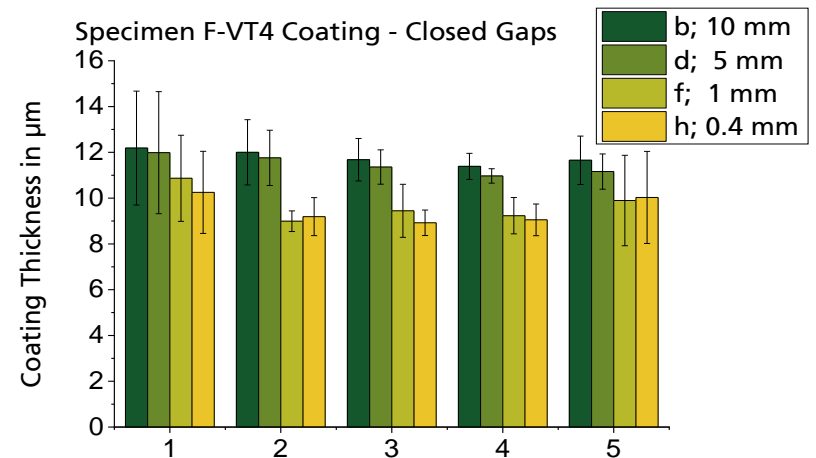
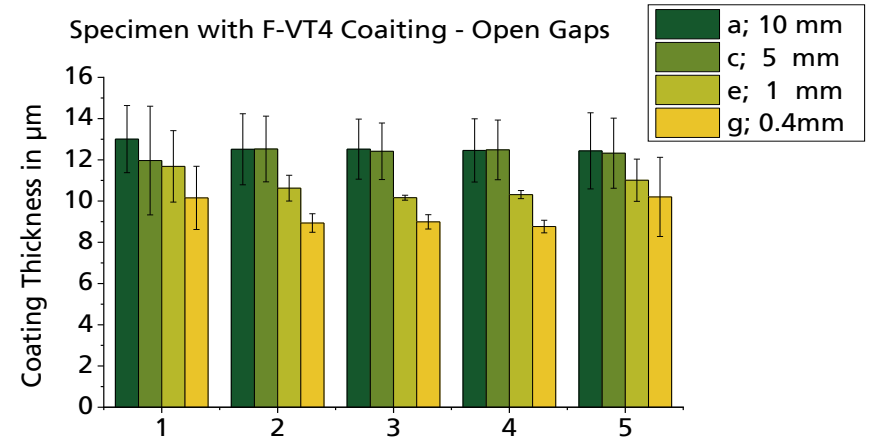


DCB test structure
(preliminary test)

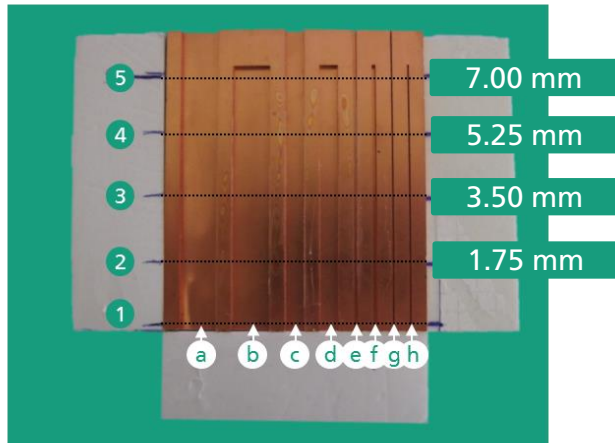
Results: Gap Filling Capability – Copper Gap Samples Parylene F-VT4 Samples



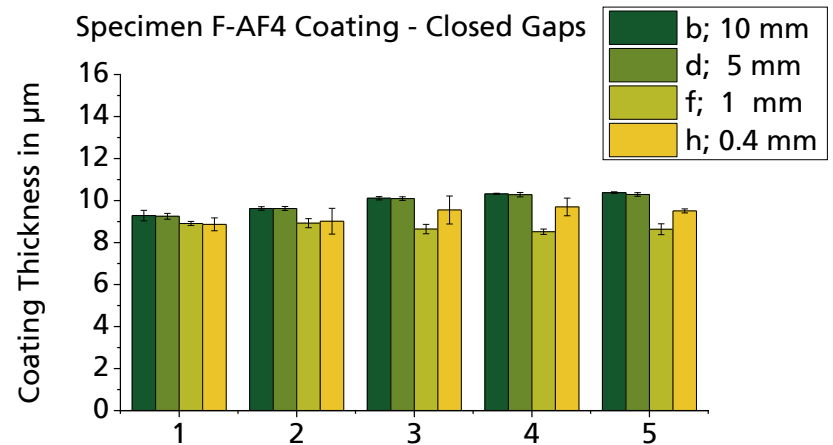
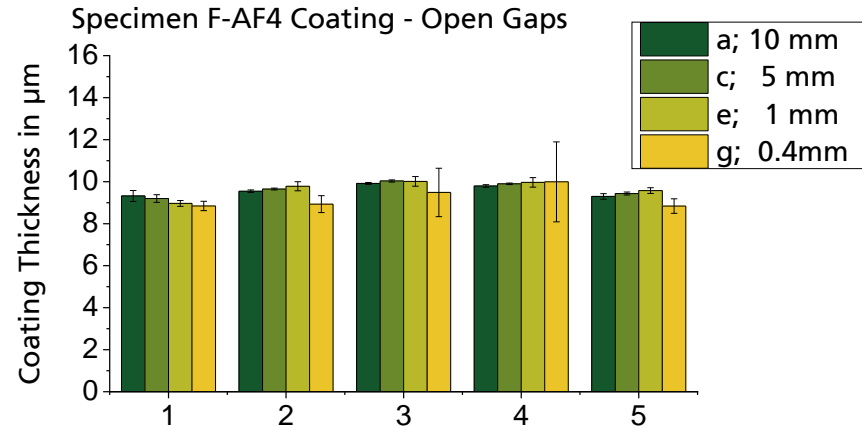
→ Successful F-VT4 coating inside all tubes of the copper gap samples
 → No decrease in layer thickness with increasing depth



Results: Gap Filling Capability – Copper Gap Samples Parylene F-AF4 Samples



→ Successful F-AF4 coating inside all tubes of the copper gap samples
 → No decrease in layer thickness with depth
 → Less scattering than with the F-VT4 samples



Results: Gap Filling Capability

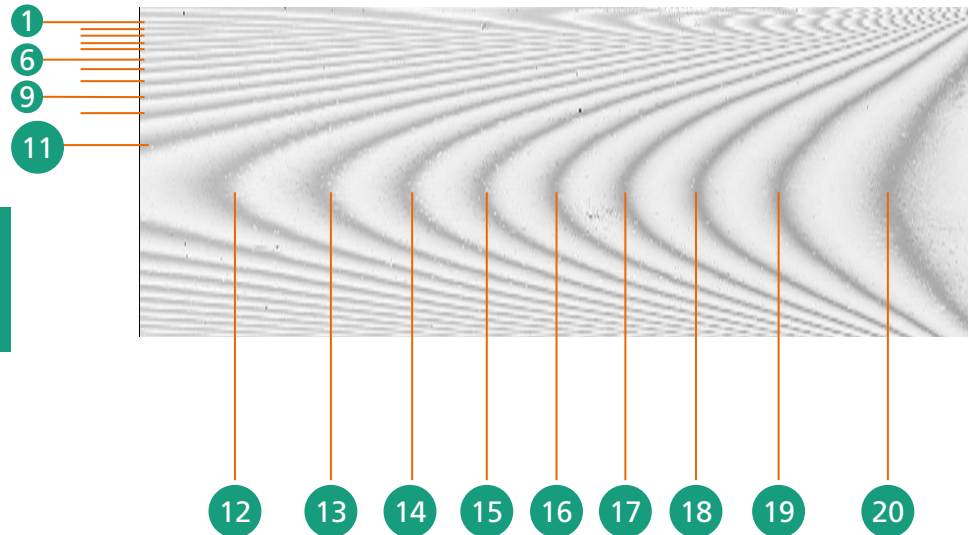
Silicon Wedge Samples – Analytical Examination

- Newton-Rings:
- Interference at wedge shaped layers
- Layer thickness on the rings is the same
- Layer thickness difference between rings:

$$\Delta d = \frac{2\lambda}{4n} = \frac{2 \cdot 780 \text{ nm}}{4 \cdot 1.559} = 0,25 \mu\text{m}$$

With:

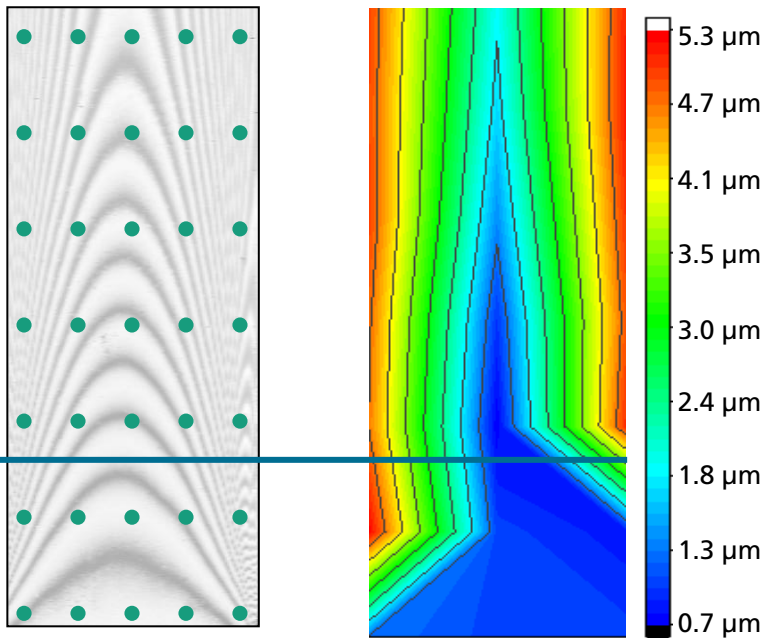
- Wavelength (Nanofocus): $\lambda = 780 \text{ nm}$
- Refractive index parylene F-AF4: $n = 1.559$



Picture of half silicone wedge sample with confocal laser scanning microscope $\mu\text{scan CF4 nanofocus}$

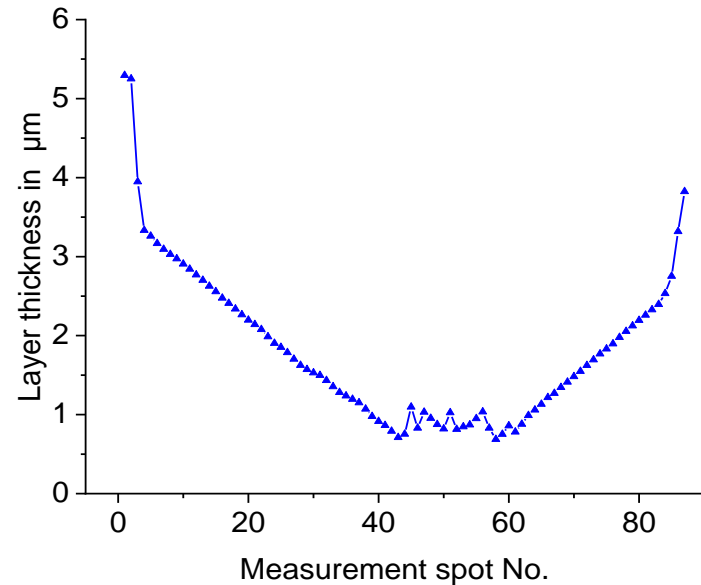
Results: Gap Filling Capability

Silicon Wedge Samples - Reflectometer Measurements



Measurement points

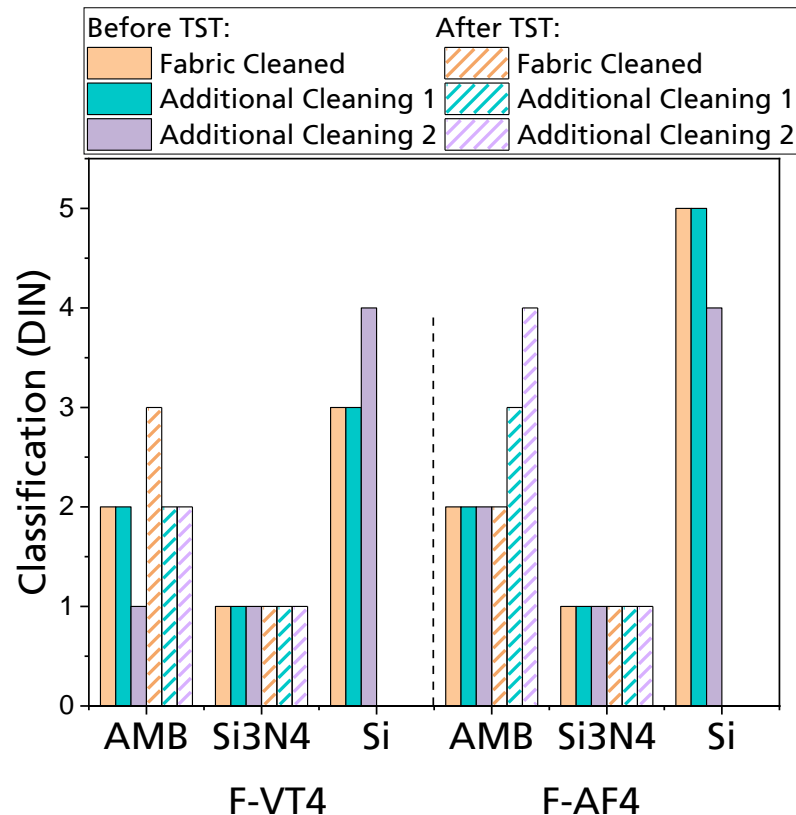
Layer thickness distribution approximated by measurement points



Layer thickness measurement along line in left figure

- Measured coating thickness distribution on sample 1 similar as expected
- At the edges the layer thickness is highest at approximately $5\mu\text{m}$
- towards the center and towards the closed side the layer thickness decreases and shows minima of approx. $1\mu\text{m}$

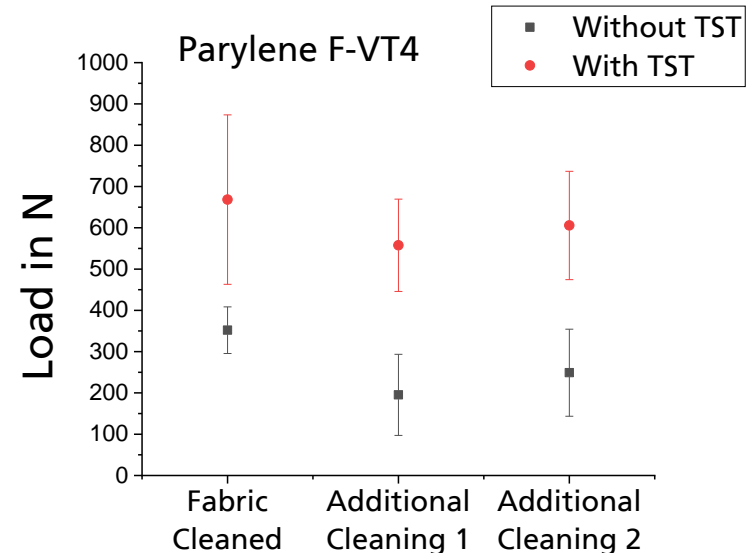
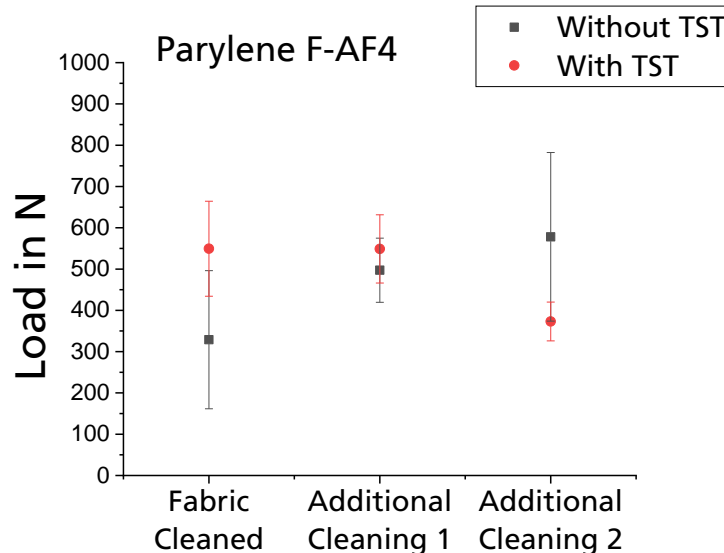
Results: Adhesion of Parylene Coatings Cross-Cut Testing



Percent Area Removed	0%	< 5%	5-15%	15-35%	35-65%	> 65%
Appearance						--
Classification (DIN)	0	1	2	3	4	5

- Highest adhesion on Si₃N₄, then on AMB, on silicon very low adhesion. This is plausible due to the surface roughness.
- On Si₃N₄ there was the same adhesion after TST as before
- Better adhesion of F-VT4 than of F-AF4 on Si
- Influence of additional cleaning different for parylene F-AF4 and F-VT4 adhesion
- Cleaning will be subject of further research and optimisation

Results: Adhesion of Parylene Coatings on AMB – Pull Shear Testing

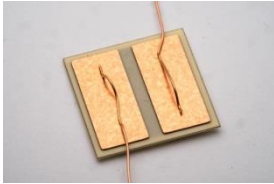


→ Additional cleaning did not make any significant difference for the measured load before TST
→ For the samples which were in the TST there was no significant change in the measured load

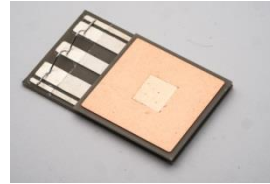
→ Additional Cleaning did not make any significant difference for the measured load
→ For the samples which were in the TST the measured load was even higher than before

Possible Explanation for the higher load after TST: change in the material characteristics of the Parylene F-VT4 Coatings

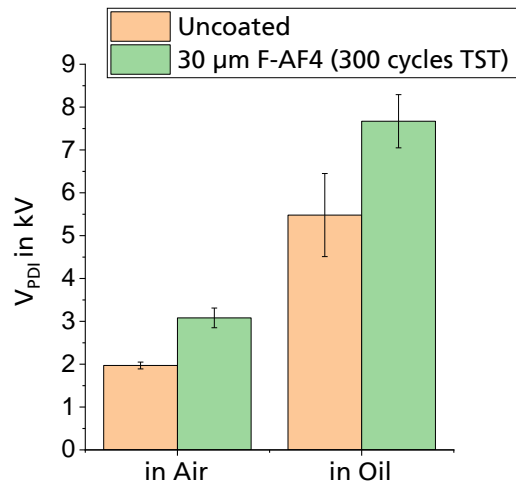
Results: Partial Discharge Measurements in Air and Oil, Uncoated and Coated



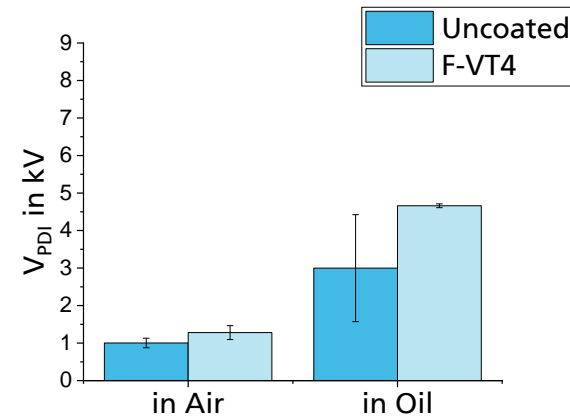
AMB test structure



DCB test structure (preliminary test)



V_{PDI} of 30 μm F-AF4 Parylene coated AMB test structures, fabric cleaned



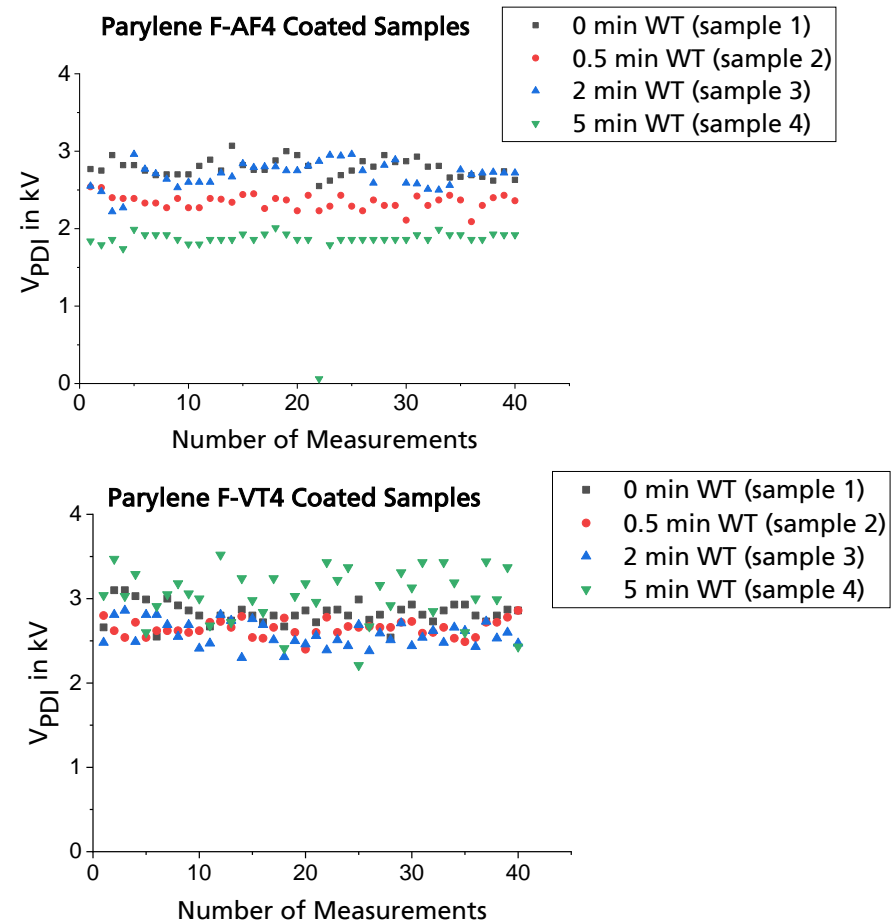
V_{PDI} of 30 μm Parylene F-VT4 coated and uncoated Ultimo samples

→ Very little difference between coated and uncoated samples in air
 → Influence of air between the coated sides will be subject of further research

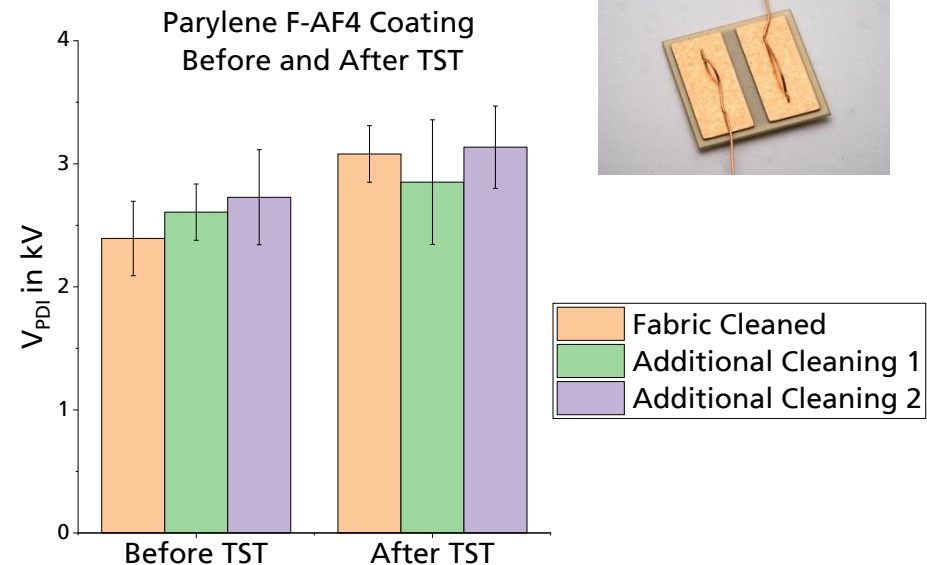
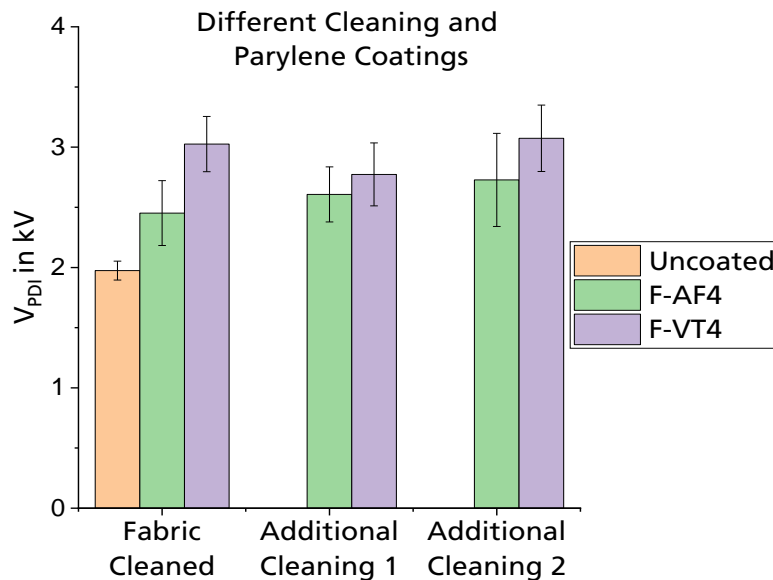
Results: Partial Discharge Measurements

40 Repeat Measurements with different Waiting Times

- As a measurement analysis for the AMB test samples with 1 mm insulation gap and 30 μm coating thickness partial discharge measurements for 8 samples with 40 instead of 5 repetitions were done
- Partial Discharge Inception Voltage (PDIV) was similar in the course of the repeated measurements for each sample
- The waiting time between the partial discharge measurements did not have influence
- Variation between the samples of each sort can be observed



Results: Partial Discharge Measurements 30 μm Coated AMB Test Structures (in Air)



- Additional Cleaning did not change partial discharge inception voltages significantly, but tendency for parylene F-AF4 coated samples were higher PDIV for additional cleaning
- Tendency of higher PDIV for parylene F-VT4 coated samples than for F-AF4 coated ones

After 300 cycles TST:

- Similar partial discharge inception voltage values for the parylene F-AF4-coated samples
- All the parylene F-VT4 coated samples had an electrical breakthrough

Summary and Outlook

- *Gap filling capability* testing shows promising results for application in DSC modules → Tests with other geometries will follow
- *Adhesion Testing:*
 - *Cross-cut testing*
 - Higher adhesion on rougher surfaces
 - Same adhesion after TST for Si₃N₄ samples, for most AMB samples less adhesion after TST
 - *Pull-shear testing*
 - Resulted in no significant change of measured load after TST for Parylene F-AF4 coated samples
 - Higher measured loads after TST for Parylene F-VT4 coated samples (changed material characteristics)
- *Partial Discharge Measurements:*
 - Showed Parylene-F-AF4 coated samples can withstand chosen TST conditions whereas Parylene F-VT4 coated ones cannot.
 - Will be further investigated for DSC samples
- Further environmental tests are yet to come: salt spray testing, corrosive gas testing, power cycling, ...
- Tests on real modules are planned

Acknowledgements

- International Clint initiative program for scientific joint research between Japan and Germany. Project IsoGap is part of this public funding.
- Ceramic circuit carrier samples were manufactured by Rogers Corporation,
- Cleaning of the samples was done by Zestron
- Coating by Plasma Parylene Systems GmbH

Thank you for your attention!