SiC MOSFET with a self-aligned channel defined by shallow source-JFET implantation: a simulation study

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Introduction

- Large cell density within a power device is needed to obtain low on-state resistance.

- Cell integration is limited by resolution and overlay accuracy of photolithography.

- Self-aligned processes, e.g. the self-aligned channel for SiC MOSFET using an over-oxidized polysilicon implantation mask [1], help to downscale the cell pitch and to increase the cell integration in the device.

Aim of this work:

- The aim of this work is to verify by TCAD simulation a new concept of the self-aligned channel process for SiC MOSFET, which uses one shallow source-JFET implantation to define the channel length.

Experimental

Concept

a) channel implantation
- in full active area (AA)
- misalignment in termination area (TA) irrelevant

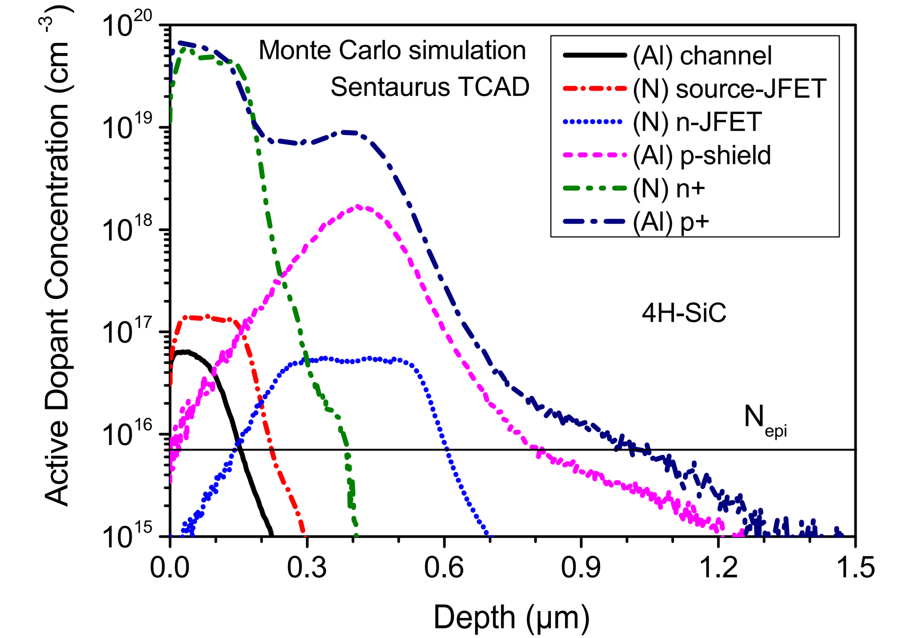
b) n-JFET implantation
- in full active area
- misalignment in termination area irrelevant

c) source-JFET implantation
- channel length (ch) defined by mask pattern

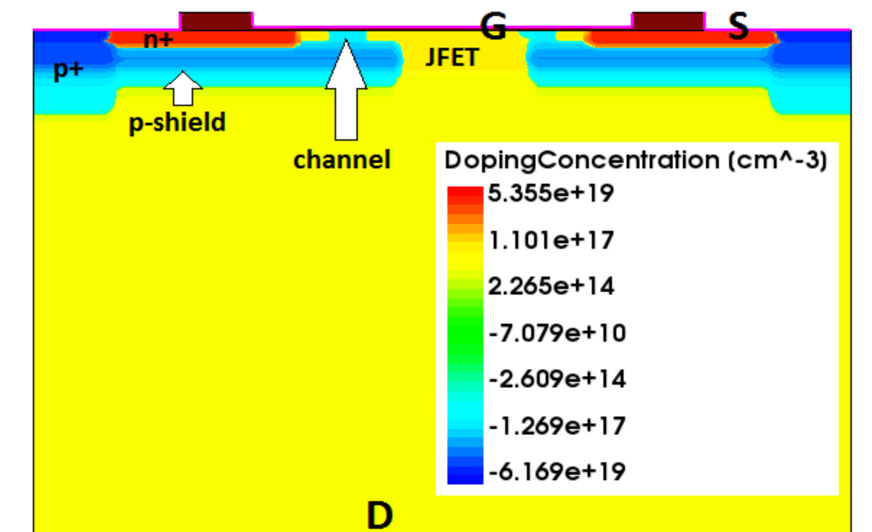
d) p-shield implantation
- alignment with channel relevant
- misalignment in termination area irrelevant

e) n+ and p+ implantation
- misalignment in active and termination area irrelevant

Simulated profiles of ions (Sentaurus)



Simulated device structure (Sentaurus)



Simulation splits

- n-JFET implantation
- JFET length J
- Misalignment between channel and p-shield
- p-shield (JFET) spacing

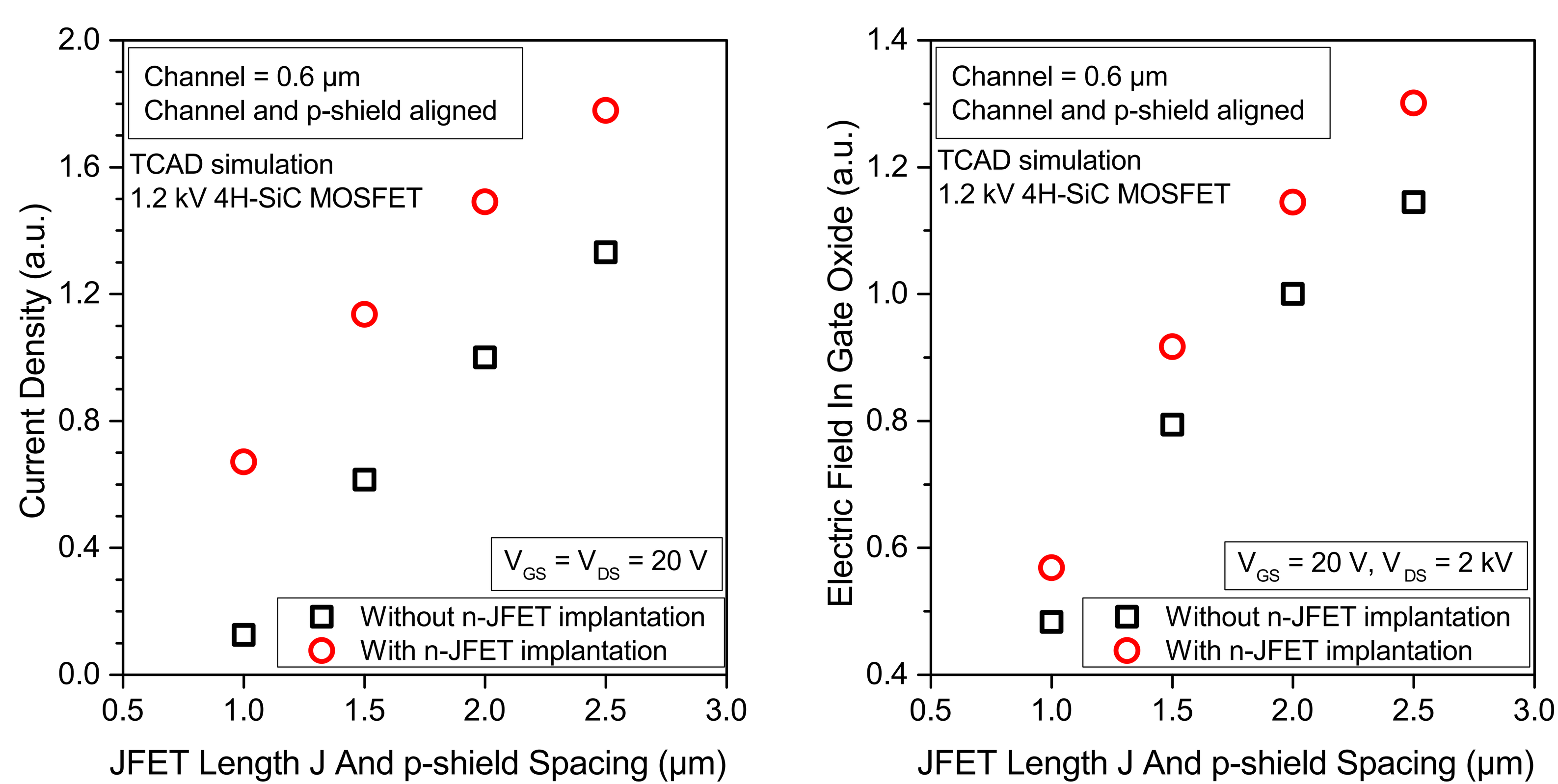
Device simulation

- Electric current in forward conduction state
- Electric field in gate oxide and drain-source leakage current in blocking state

Results

1. n-JFET implantation

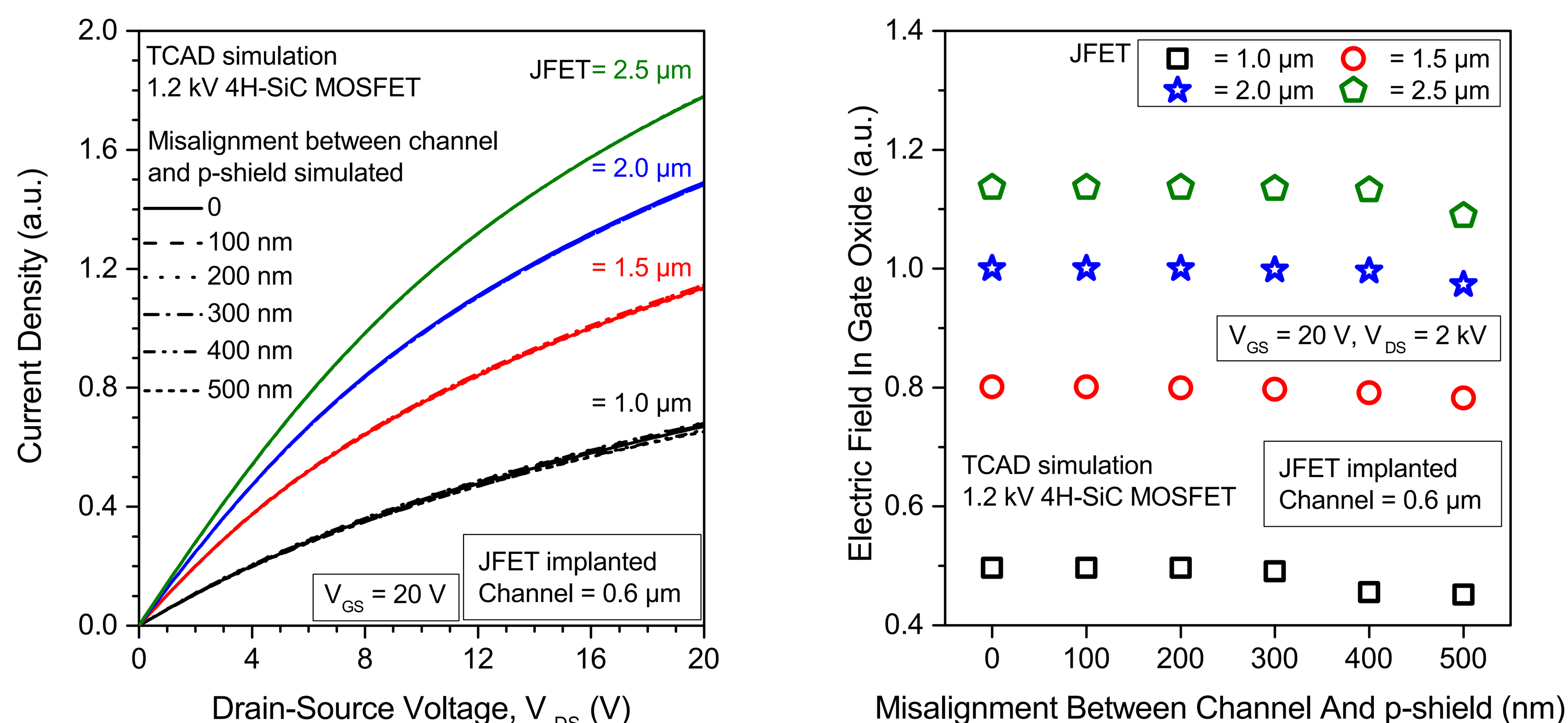
- Increase of forward current density and electric field in gate oxide in blocking state due to n-JFET implantation



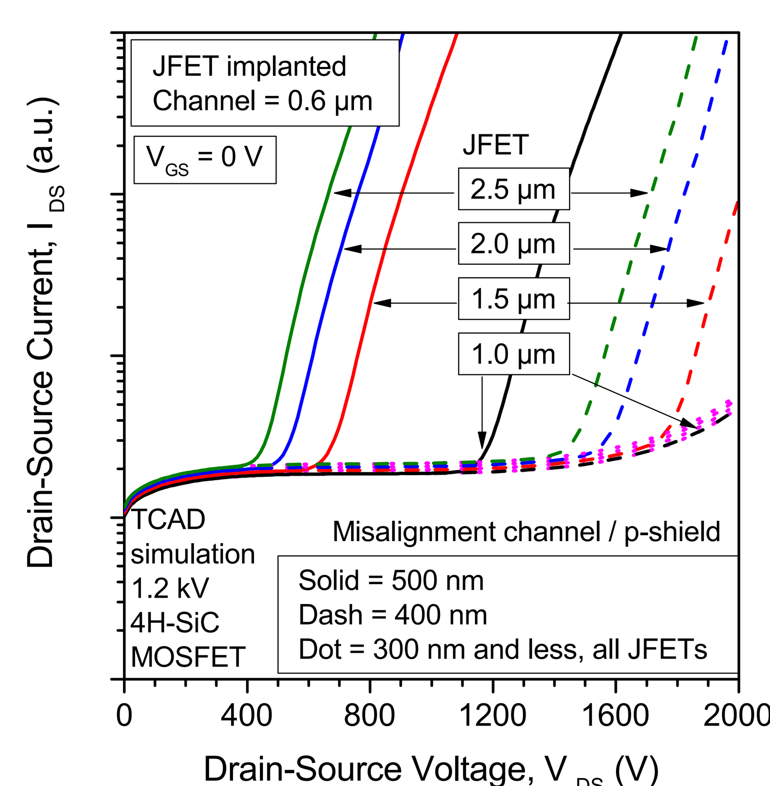
2. Misalignment between channel and p-shield

- No impact of misalignment up to 500 nm on forward current density, for all simulated JFET lenghts

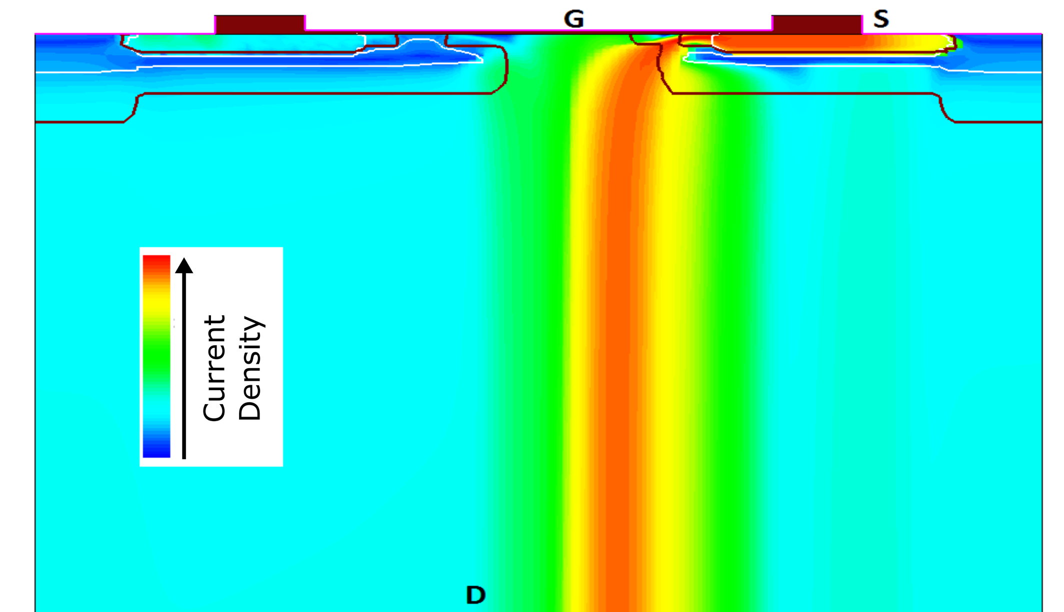
- No impact of misalignment up to 300 nm on electric field in gate oxide in blocking state, for all simulated JFET lenghts



- Increase of leakage current between drain and source in blocking state for 400 nm and 500 nm misalignment, dependent on JFET length



- Example: increase of leakage current between drain and source in blocking state for a 4H-SiC MOSFET with JFET = 2 µm and misalignment between channel and p-shield = 500 nm



Conclusions

- Based on the TCAD simulation, a new concept of a self-aligned channel defined by shallow source-JFET implantation is applicable to fabrication of functional SiC Power MOSFET. This method could be used for fabrication of devices with short channel and reduced on-state resistance.

- A critical process step is the alignment between channel and p-shield layers. The misalignment betweeen channel and p-shield has to be well controlled. For simulated JFET lengths and 0.6 µm channel, it should be smaller than 400 nm, in order to achieve robust devices.

- With some modification and additional processing, the process could be used for fabrication of SiC MOSFET with an epitaxial channel, for which the aluminum implanted channel layer is replaced with a thin lightly-doped p-type epitaxial layer.

References

[1] M. Matin, A. Saha and J. A. Cooper, IEEE Transactions on Electron Devices, Vol. 51 (2004) 1721.