Benchmarking experiment of substrate quality including SmartSiC™ wafers by epitaxy in a batch reactor

B. Kallinger[1)], P. Hens[2)], P. Berwian[1)], C. Kranert[1)], K.M. Albrecht[2)], J. Erlekampf[2)]
[1)] Fraunhofer IISB, Schottkystraße 10, 91058 Erlangen, Germany
[2)] AIXTRON SE, Schottkystraße 10, 91058 Erlangen, Germany

E-mail: Birgit.Kallinger@iisb.fraunhofer.de (corresponding author)

To produce Silicon Carbide (4H-SiC) power electronic devices, conventional 4H-SiC substrates with 150 mm diameter and 350 µm thickness are currently widely used, which can be purchased from many vendors worldwide. Today, they are still an essential part in the cost structure of power electronic devices as the production of such 4H-SiC is expensive. Moreover, today's SiC substrates contain structural defects, which are inherited to the epilayer and hence, the active device area, where they can limit the device performance and production yield.

Using a very thin 4H-SiC layer could be sufficient for epitaxy and device production and the defectivity of the epilayer could also be improved. In addition, the device performance can be strongly enhanced thanks to lower device conduction and/or switching losses using ultra high conductivity receiver substrates. SOITEC's Smart Cut™ process [1] yields such a 0.6 µm thin SiC layer, which is transferred to a polycrystalline SiC carrier substrate and bonded thanks to a conductive bonding, called SmartSiC™ substrate. Defects in epilayers on such SmartSiC™ substrates can then have three different origins: 1) inherited from the conventional substrate, 2) originate from the Smart Cut™ and layer bonding processes, and 3) originate from the epi growth itself. This paper aims to investigate the current quality of epilayers grown on SmartSiC™ substrates and identify the origin of defects. Therefore, SmartSiC™ and conventional 4H-SiC substrates are benchmarked in a comprehensive epitaxial study in the framework of the TRANSFORM EU project.

The benchmark study comprises SmartSiC™ substrates of 4H-SiC donor wafer bonded onto 4H-SiC handler (in this paper named Gen1.1), 4H-SiC bonded onto poly-SiC (in this paper named Gen1.2) and conventional substrates from STMicroelectronics as partners in the TRANSFORM project as well as other international suppliers (vendor A with prime and engineering grade, vendor B with prime grade). All substrates are n-type and 150 mm in diameter. All SmartSiC™ substrates contain a conductive bonding layer, the Gen 1.1 substrates a monocrystalline 4H-SiC carrier wafer and the Gen 1.2 a polycrystalline SiC carrier wafer. The SiC top layers of the SmartSiC™ substrates compare well to the conventional substrates provided by STMicroelectronics, hence, we can conclude which defects in the epilayer originate from the substrate material. To investigate if the Smart Cut™ process introduces additional defects to the epilayer and if the epi growth process needs further optimization for SmartSiC™ substrates, conventional substrates from different international suppliers are added.

All prime grade non SmartSiC™ substrates have been characterized prior to epi growth by x-ray topography (XRT) with a Rigaku XRTmicron [2] and all have been measured with UVPL imaging and surface inspection with a Lasertec SICA88 and Intego AQUILA systems. Then, a sequence of epi growth runs has been started in an AIXTRON G5 WW C planetary reactor in 8x150 mm configuration: 1) a standard epi growth process including buffer growth and standard epilayer; 2) a buffer only growth; and 3) a heat-up and cool-down procedure with thermal etching at process temperature. During the epitaxial growth process in-situ data of temperature profiles and wafer curvature was recorded. All wafers with grown layers were then characterized regarding epilayer thickness and doping concentrations by FTIR spectrometry and mercury probe CV measurements, respectively. All wafers are being characterized using UVPL imaging plus DIC/optical microscopy and all full stack epilayers with XRT for defectivity after the epitaxial process or thermal etching. We will show and discuss the growth and characterization results and compare the performance of conventional and Smart SiC substrates.

[1] S. Rouchier *et al.*, "150 mm SiC engineered substrates for high-voltage power devices", ECSCRM 2021
[2] Rigaku XRTmicron (not a standard characterization method like UVPL imaging)