Presented at the 23rd European Photovoltaic Solar Energy Conference and Exhibition, 1-5 September 2008, Valencia, Spain

REAR-SIDE CONTACT STRUCTURE FOR EPITAXY WRAP-THROUGH SILICON THIN-FILM SOLAR CELLS

E.J. Mitchell[1,2], M. Künle[1], M. Kwiatkowska[1], S. Janz[1], S. Reber[1]
[1]Fraunhofer Institute for Solar Energy Systems, Heidenhofstrasse 2, 79110 Freiburg, Germany,
[2]School of Photovoltaic and Renewable Energy Engineering, UNSW, Sydney, 2052, Australia,
Corresponding author: Emily Mitchell, Tel.: +49 761 4588 5390, Fax.: +49 761 4588 9250
E-mail: emily.mitchell@ise.fraunhofer.de

ABSTRACT: The Epitaxy Wrap-Through (EpiWT) cell is a rear contact version of the Epitaxial Wafer-Equivalent, our crystalline silicon thin-film solar cell. The EpiWT concept is similar to an Emitter Wrap-Through cell but the rear structuring requires an isolation layer. Amorphous silicon carbide layers have been tested using an experimental sample structure. The layer resistivity and pinhole incorporation were measured using different types of metal contacts, and laser-scribed isolation trenches were demonstrated. The results indicate that SiC would be a suitable isolation layer for the EpiWT cell if applied with evaporated metallisation, but the laser trenches require further optimisation.
Keywords: back contact, silicon carbide, laser processing

1 INTRODUCTION

The Epitaxy Wrap-Through (EpiWT) cell is a new thin-film solar cell concept under development at Fraunhofer ISE. Its purpose is to enable rear-side contacting for 'Wafer-equivalents', which are our epitaxial thin-film silicon solar cells. The structure employed resembles that of an Emitter Wrap-Through (EWT) cell, except that all of the active layers are wrapped through the via holes, not just the emitter.

Development work is underway on several novel process steps that will be involved in producing EpiWT cells. These include laser structuring of the substrate, epitaxial deposition directly through the via holes, formation of a rear-side isolation layer and structuring of an interdigitated rear-side metallisation. This paper focuses on the experimental investigation of one possible rear-side structure using a silicon carbide isolation layer and a laser-structured interdigitated metallisation.

2 BACKGROUND

2.1 Wafer-equivalents

The epitaxial 'Wafer-equivalent' silicon solar cell combines the advantages of thin-film and thick-film solar cell technologies. It consists of a low-cost, highly-doped (0.02 Ωcm) silicon substrate upon which the thin, active layers of the solar cell are epitaxially grown. The name 'wafer-equivalent' is given because the structure behaves like a standard wafer solar cell and can therefore be metallised in the same way. The thin-film advantage is gained through the reduction in expensive, high-grade silicon consumed. The thick-film advantages that are retained include excellent silicon crystal quality and a wealth of directly applicable and well-developed metallisation techniques.

2.2 Rear-side contacts

There are several motivations to develop rear-side contacting for Wafer-equivalents. The primary incentive is to increase current collection, which is reduced by up to 8% due to reflection from front-side metallisation. Light trapping is particularly important for thin-film solar cells because light absorption decreases with a shorter path length through the silicon. Accordingly, in the Wafer-equivalent cell results thus far, it is the current density (~ 30 mA/cm^2 in a 20-µm layer) rather than the voltage (~ 650 mV) which shows the greater potential for improvement [1]. Further advantages of rear-side contacts include easier module fabrication and increased module efficiency due to denser cell placement.

3 THE EPITAXY WRAP-THROUGH CELL

The epitaxial base and emitter layers of the EpiWT cell cover the front surface and wrap through the via holes to the rear surface. This structure is directly grown using high-temperature APCVD (atmospheric pressure CVD) in a chamber that is primarily designed for single-sided processing. The initial results of this epitaxy-through-holes deposition process have been described elsewhere [2].

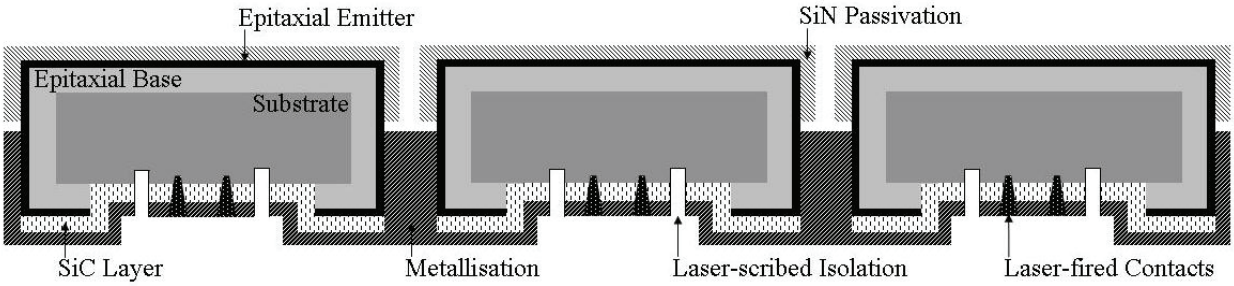

Figure 1: Cross-section diagram of the EpiWT cell structure, in this case with an SiC layer serving as isolation.

Before discussing possible metallisation schemes for the EpiWT cell, the structure must be closely analysed. The essential element of the structure is that the base and emitter layers cover the front surface and the inner surfaces of the via holes, but extend only a short way over the rear surface (that is, a given radius from the holes). This must be so to avoid voltage loss caused by the non-illuminated rear-side junction [3]. Consequently, compared with the normal EWT cell, there is an important difference in the required rear-side structuring. In a normal EWT cell, the rear surface of the silicon wafer is structured with interdigitated emitter and base regions to match the interdigitated metallisation, thus preventing shunts. In the EpiWT cell, an isolation layer is necessary to separate the metal emitter contact finger from the p-type substrate.

3.1 SiC Isolation Layer

One possible implementation of the metallisation for the EpiWT cell structure is shown in cross-section in Figure 1. Here the isolation is achieved with an amorphous silicon carbide (a-SiC:H) layer. SiC is being pursued because of its excellent diffusion barrier characteristic and disruptive strength [4]. The challenge is to deposit a pinhole free layer. In principle this can be achieved with low growth rates at highest possible temperatures and at high plasma densities. Any contaminations of the surface have to be avoided to prevent blistering and other layer interceptions.

The SiC layer is deposited over the rear surface of the cell after the epitaxy process. This layer covers the exposed rear surface of the p-type substrate but leaves the n-type emitter surface in the holes available for contacting. A continuous metal layer is applied by some means, most likely screen printing or evaporation, over the entire rear surface and inside the holes.

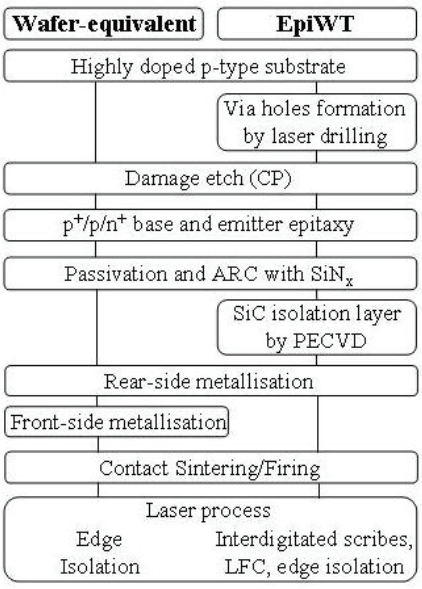

Figure 2: Process sequences for the Epitaxial Wafer-Equivalent and the Epitaxy Wrap-Through solar cells.

This metal layer is subsequently structured using laser processing, taking advantage of the non-critical rear surface of the EpiWT cell. To create an interdigitated contact, two tasks must be completed; trenches are scribed to isolate the p and n contact fingers from each other and laser-fired contacts (LFC) are formed to connect the p contact fingers to the substrate. Alignment problems are completely avoided by this approach because both of these steps can be done in the same laser process. The substrate can be damaged without detriment to the cell performance, which means that the laser parameters can be optimised purely to benefit the contact quality. However, an additional wet-chemical etch may be required to ensure proper isolation in the laser trenches.

In comparison to the standard wafer-equivalent process sequence, this implementation of the EpiWT cell only requires two additional steps – the via hole drilling and the SiC layer deposition. Furthermore, the front-side metallisation step is no longer necessary. A comparison of the two process sequences is shown in Figure 2.

4 EXPERIMENTAL

4.1 Sample Structure and Processing

An experimental test structure was developed to assess the performance of the SiC isolation layer and the laser processing (see Figure 3). The geometry and processing were made as similar as possible to the rear-side of the envisaged cell structure, but the measurement was greatly simplified by the absence of the epitaxial layers and pn-junction.

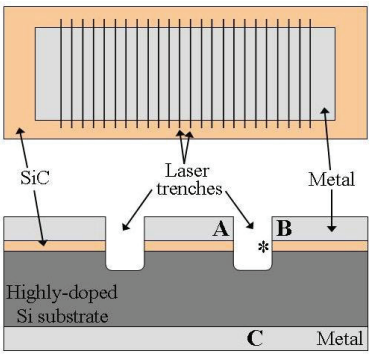

Figure 3: Top view (top) and cross-section view (bottom) of the experimental test structure.

The substrate used was highly-doped (0.02 Ωcm), multicrystalline silicon, prepared with a chemical polish (CP) damage etch. Intrinsic, amorphous SiC layers were deposited by PECVD in four separate depositions with parameters as shown in Table 1. The first two depositions both used a well-tested, standard SiC process recipe, just with different layer thicknesses. The third was a repeat of the thicker layer with this same standard recipe, but a few months later. On the same day the fourth deposition was also performed, using a newly developed, denser layer. The deposition temperature and plasma density were higher, resulting in a lower hydrogen concentration in the layer.

Table 1: Summary of the SiC layer depositions that produced all of the experimental test samples.

Deposition	When	Type	Thickness
#1	First day	Standard	100 nm
#2			300 nm
#3	2 months later	Standard	300 nm
#4		Dense	200 nm

Metal was applied using either evaporation or screen-printing with various pastes. The evaporated metal stack consisted of three layers, namely 300 nm Al, 20 nm Ti and 100 nm Ag. This combination is not significant, rather the process was chosen as it was transferred from some other work. The evaporated metal was sintered at 300°C for 10 minutes. Three screen-print pastes were trialled: Al, standard Ag and low-frit Ag. The printed metal was fired at 900°C. Note that the evaporated metal was first tested on samples from the later depositions.

Isolation trenches were laser-scribed through the metal and SiC layers. The laser process had to produce a clean trench, free of metal debris. A frequency-tripled Nd:YVO4 laser was used and the parameters varied were the focus, the pulse spacing and how many times a trench was scribed.

Additionally, some samples were etched with wet chemistry to remove metal debris and improve the isolation properties. HNO_3 was used for the silver screen-printed metal (concentration between 20% to 70% and etch time 5 to 60 seconds) and a buffered Aluminium etch solution containing phosphoric acid, nitric acid and acetic acid for the evaporated metal (1 minute).

4.2 SiC Layer Resistance Measurement

The performance of the SiC as an isolation layer depends on the resistivity of the material as well as the mechanical properties of the layer (e.g., lack of pinholes). Hence, the test structure was designed to allow assessment with regard to both factors. The layer resistances were first measured over the entire sample area before the laser trenches were scribed, and afterwards over the small areas between the trenches.

The resistance was measured from the top metal contact to the bottom metal contact. The bottom metal contact was added solely to enable measurement and did not affect the SiC layer. The size of the top metal contact was known (5.6 cm^2) and hence the specific resistivity of the SiC could be calculated. However, this calculated quantity is not so relevant if there are pinholes in the layer, because the necessary assumptions no longer hold. In this case, the quantity is useful for comparison of resistance measurements over different areas, but should not be interpreted as a reliable indication of the SiC material specific resistivity.

4.3 Laser-trench Resistance Measurement

The aim of the laser scribing was that the narrow (1-mm wide) metal strips created would be isolated from each other. Logically, a direct resistance measurement from one strip to the next (e.g., from point A to point B in Figure 3) should be an appropriate indicator of performance. However, because the substrate is conductive, the resistance between these strips can only be as good as the resistance through the SiC layer. Furthermore, the point marked with an asterisk (*) in Figure 3 on the sidewall of the trench is the only point where a shunt matters, again because the substrate is conductive anyway. The SiC layer is very thin in comparison to the metal layer, so a piece of ablated metal could easily form a 'bridge' across it. This means that a front-to-back measurement through the SiC layer in the laser-scribed section is a better test of the isolation scribe. Indeed, it was experimentally confirmed that the resistance between points A and B is always just the sum of the resistances from points A to C and from points B to C. The scribe spacing was 1 mm and the width of the metal contact was 1.4 mm so the resultant strip area was 0.14 cm^2.

5 RESULTS

5.1 SiC Layer Resistance Results

The results of the resistance measurements through the standard SiC layers are shown in Table 2. The performance of the layers varies greatly with the different types of metal and the different thermal processing steps. The SiC layer was not penetrated by the evaporated metal layer. The measured resistance up to 8 MΩ, when given the layer area and thickness, correlates to a specific resistivity of 1.5 x 10^{12} Ωcm, which is in the upper end of the known range of resistivity values for SiC [5]. The outcome of the subsequent sintering of these layers demonstrates their high potential, because the layer resistance of some samples (labelled 'good SiC' in Table 2) actually increased from the sintering, by up to a factor of 10. This is to be expected, as thermal processing increases the layer density by allowing some hydrogen to escape, resulting in the formation of more high-bandgap SiC bonds [5]. However, on other samples (labelled 'faulted SiC' in Table 2) from the same deposition and even cut from the same wafer, the resistance drastically decreased. This indicates faults or imperfections in the layers, which the metal takes advantage of during the thermal processing.

The effect of screen-printed and fired metal on the SiC layer was, all in all, more damaging, although again the extent to which the layers broke down varied with the metal type. The most catastrophic SiC layer breakdown occurred with screen-printed and fired Aluminium. The measured resistances were in the range of mΩ which is purely the resistance through the highly-doped silicon substrate, showing that the isolating SiC layer was completely compromised. Similar effects, though less drastic, were observed with the silver screen-printed metal. The ability of the silver paste to fire through the SiC depended on the paste composition, specifically the glass frit content. As is to be expected, the SiC layers were less attacked by the low-frit silver paste than the standard paste.

Table 2: Results of resistance measurements through standard SiC layers (from deposition #3), with various metal layers, 5.6 cm^2 area.

Metal	Thermal processing	Sample Size	Average resistance *(std. dev.)*	Best resistance
Evaporated	-	30	2.3 MΩ *(1.9 MΩ)*	8 MΩ
Evaporated (good SiC)	Sintered 300°C	5	20.7 MΩ *(11.2 MΩ)*	30 MΩ
Evaporated (faulted SiC)		5	4.1 kΩ *(5.4 kΩ)*	14 kΩ
SP Ag std.	Fired 900°C	30	1.2 Ω *(0.7 Ω)*	3.2 Ω
SP Ag Low-frit		30	4.0 Ω *(2.1 Ω)*	9.0 Ω
SP Al		33	2.6 mΩ *(0.3 mΩ)*	3.3 mΩ

Besides the sensitivity to metal type and thermal processing, the layer performance varied for the different SiC depositions (refer back to Table 1 for deposition overview). The results in Table 3 show a comparison of the SiC layer performance with screen-printed Ag from the four depositions. Apparently, the third standard deposition was better than the first two, probably due to the state of the PECVD deposition system at the later date. For example, it is known that the chamber cleanliness or the presence of dopants from preceding processes affect the properties of the deposited layers. Additionally, flaking from deposited material on the chamber walls can disturb homogeneous layer formation and create pinholes if the particles land on the sample. In any case, the measured resistances from the first depositions were lower than those from the third, by up to one order of magnitude. Also note that the resistance values for the first two depositions vary roughly proportionally to the layer thickness.

Regarding the denser layer of deposition #4, from analysis of the screen-printed samples, it seemed that it was a little better, though not significantly. Also looking at the evaporated metal samples, the denser layers seemed promising before sintering. However, the sintering process exposed the structural flaws of the layers; a large drop in resistance values was seen. Whereby the resistance of the standard SiC samples with evaporated metal on average either dropped to 4 kΩ or rose to 20.7 MΩ (due to the presence or absence of SiC-layer imperfections) after sintering, the dense SiC sample values all dropped to, on average, 500 Ω.

Table 3: Results of resistance measurements through SiC layers from various depositions, all with standard screen-printed silver metal layers, 5.6 cm^2 area.

Deposition	Thickness	Sample Size	Average Resistance *(std. dev.)*	Best resistance
#1 Std.	100 nm	10	0.10 Ω *(0.07 Ω)*	0.23 Ω
#2 Std.	300 nm	27	0.20 Ω *(0.05 Ω)*	0.32 Ω
#3 Std.	300 nm	30	1.2 Ω *(0.7 Ω)*	3.2 Ω
#4 Dense	200 nm	30	1.3 Ω *(0.9 Ω)*	3.8 Ω

5.2 Laser-trench Resistance Results

The best results of the resistance measurements from the laser-scribed, front contact strips through to the rear contact are shown in Table 4.

Table 4: Best results of resistance measurements through SiC layers on small laser-scribed contact strips, 1.4 cm^2 area.

Deposition	Metal	Wet-chem. etching	Best resistance
#2	Scr.Pr. Ag	-	900 Ω
		HNO_3	2000 Ω
#3	Scr.Pr. Ag	-	2.5 Ω
	Evap.	-	4 Ω
		Al etch	4 Ω

The best value for the as-lasered, measured resistance through the 1.4 cm^2 SiC layer was 900 Ω, but the results varied widely, right down to 1 Ω. Comparison of the calculated specific resistivity values (3.7 x 10^4 over large area to as high as 4.2 x 10^6) shows an apparent improvement of roughly two orders of magnitude from laser scribing. It isn't possible that the material resistivity actually improved. Rather, this indicates that the firing of the metal through the SiC layer was not homogeneous, and this particular strip was simply less shunted than others (although still well below the potential 10^{11} Ωcm demonstrated with the evaporated metal). A calculation which supports this theory is that the parallel combination of all the strip resistances from one sample is about 0.1 Ω, slightly decreased from the 0.4-Ω large-area resistance by the laser process. It is not possible that the laser process alone was to blame for the variability of the results because if each strip had a resistance of 900 Ω, the parallel combination would be 22 Ω, much higher than the real value. However, the laser process did contribute to the shunt, as was tested by making some samples with fewer laser scribes, i.e. 3 instead of 32. The parallel combination of the resistances of that sample was 0.3 Ω, closer to the large-area value.

The difference between the best measured resistances before and after the HNO_3 etching was not significant. The benefit of the etch process seems to be increased reliability and weaker dependency on the laser parameters. However, further efforts will be made to sufficiently optimise the laser parameters; it would be a great advantage not to require the etch step. An SiC-Ag adhesion problem was encountered during the etching. That is, the acid penetrated under the silver layer so that the layer would peel away from the surface. This occurred fairly quickly, for example after just 15 seconds in 35% HNO_3. The appearance of the SiC layer underneath had completely changed (from colourful and shiny to dark grey and matt), either from the etching or the firing.

As evident in Table 4, the repeatability of the 900-Ω result could not be demonstrated. Even though the SiC resistances were much better for the later depositions, especially with evaporated metal, the laser scribing results were disappointing. Neither the previously optimised laser parameters nor an attempted re-optimisation, including testing a pico-second laser, yielded an improvement. As of yet, no satisfactory explanation has been found. Obviously, further process development is required.

6 DISCUSSION

It is necessary to know what level of performance needs to be demonstrated on the test structure in order to prove the suitability of the design for the EpiWT cell concept. This can be calculated from some simple analysis of the planned design of the finished cell. However, the results of the calculation depend on whether the dominant problem is taken to be the metal shunting through the SiC layer or the shunting in the laser trenches. That is, the primary geometrical parameter in the calculation is different. The shunt resistance value due to shunting through the SiC layer is inversely proportionally to the layer area, whereas the value due to shunting from the laser is inversely proportional to the trench length.

This work has demonstrated that both the SiC layer resistivity and the trench shunting contribute to the overall shunt, and so both versions of the calculation are relevant. A cell size of 15.6 x 15.6 cm^2 and a desired shunt resistance of > 50 Ω are assumed. Looking first at the SiC layer resistivity and assuming the trenches are perfectly isolating: for an SiC layer thickness of 500 nm and a 50% rear-surface emitter contact fraction, the required SiC resistivity is 1.2 x 10^8 Ωcm, which equates to 645 Ω on the 5.6-cm^2 test structure. Next looking at the laser trenches and assuming the SiC layer is perfectly isolating: working back from a trench length of 1.1 m in the final cell (pitch = 2 mm), the required resistance on a test sample strip is 40 kΩ.

The demonstrated SiC layer performance with evaporated metal, even after a sintering step, is significantly better than that required to prove suitability for the EpiWT cell structure. The laser trench results are less convincing due to the high variation and the lack of reproducibility. However the best result achieved is only one order of magnitude below the required value, so with further process optimisation it should be possible to successfully scribe isolating trenches. Alternatively, SiC isolation layers could be used but with a different method to structure the metal. The LFC process is also yet to be tested, but our experience from the laser trench optimisation is that finding laser parameters to create a contact should not be difficult.

7 CONCLUSION

The new EpiWT cell concept for rear contacting of epitaxial wafer-equivalents has been explained. The suitability of silicon carbide for the isolation layer has been assessed with use of an experimental test structure. Both the resistance through the SiC with various metallisations and thermal processing steps, as well as the resistance of isolating laser trenches, has been investigated. The results show that the SiC layer resistivity is adequate if applied with an evaporated metallisation, but the layers cannot withstand fired, screen-printed metal. The laser-scribed isolation trenches have been demonstrated. However, the best measured resistance is still a little too low and the result could not be reliably reproduced, so further process development is required.

8 ACKOWLEGEMENTS

The authors would like to thank all their colleagues who contributed to this work, intellectually or practically. Special thanks go to Christian Harmel, Felix Schätzle and Marc Retzlaff for the sample processing.

Emily Mitchell gratefully acknowledges the financial support from the UNSW Faculty of Engineering through the Women in Engineering Scholarship Program.

9 REFERENCES

[1] E. Schmich, H. Lautenschlager, T. Frieß, F. Trenkle, N. Schillinger and S. Reber, Progress in Photovoltaics: Research and Applications 16 (2008) 159.

[2] E.J. Mitchell, S. Reber, Proceedings 33rd IEEE Photovoltaic Specialists Conference (2008) in print.

[3] P. Hacke, J.M. Gee, M. Hilali, J. Dominguez, H. Dundas, A. Jain, G. Lopez, Proceedings 21st European Photovoltaic Solar Energy Conference (2006) 761.

[4] S. Janz, Ph.D. Thesis, Universität Konstanz, 2006.

[5] F. Demichelis, C.F. Pirri, E. Tresso, G. Della Mea, V. Rigato, P. Rava, Semiconductor Science and Technology 6 (1991) 1141.