Robuste und zuverlässige Leistungselektronik: Umwelt- und Lebensdauertests

8. Kooperationsforum Leistungselektronik
Novum Businesscenter Würzburg

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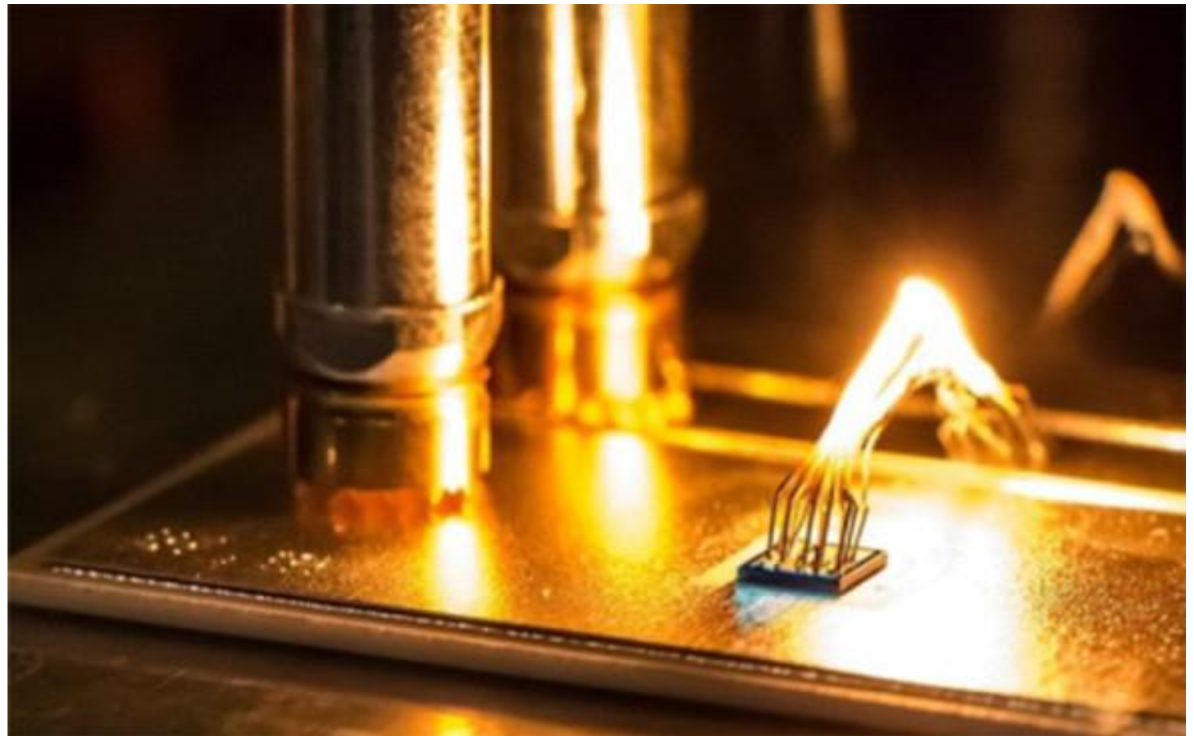

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- Definition of robustness, reliability and lifetime
- Challenges for the testing WBG
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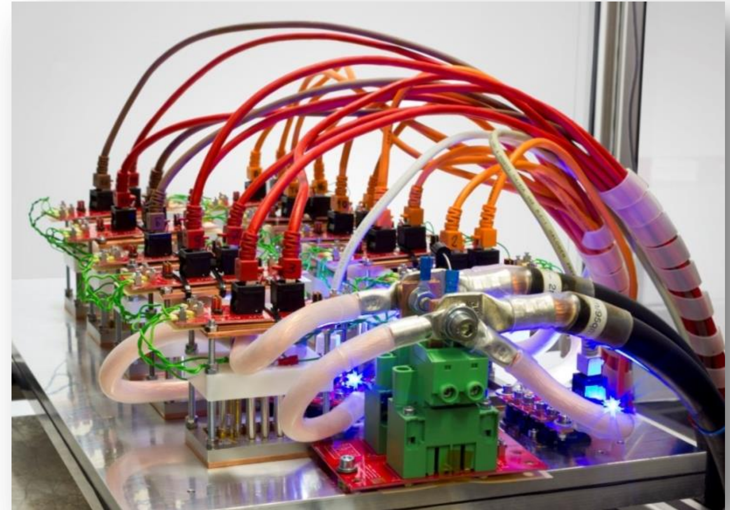

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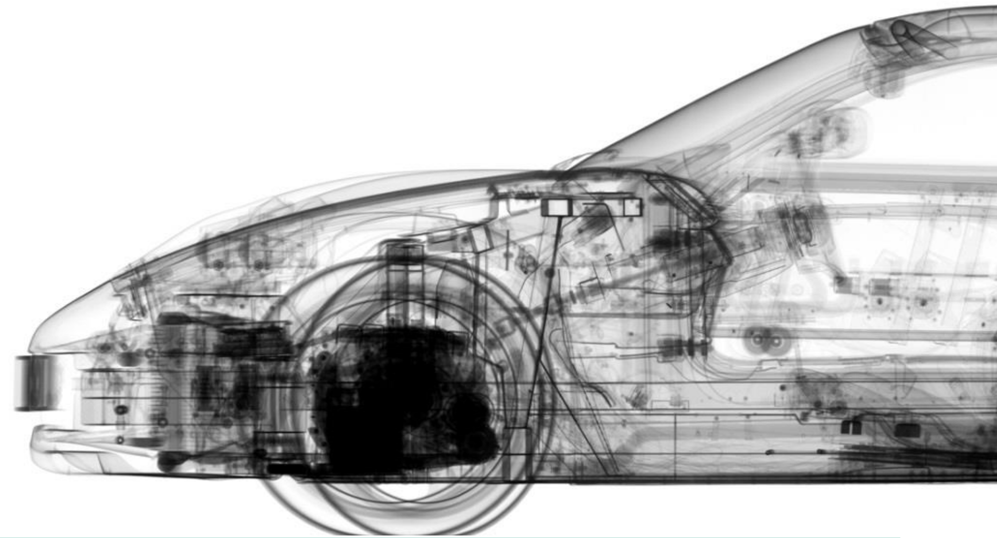
Definition

- Robustness is the probability that a product performs its intended function for a ~~specified~~ period of time under a specified set of operating conditions.
- Reliability is the probability that a product performs its intended function for a <u>specified</u> period of time under a specified set of operating conditions. (VDI guideline 4001)
- Robustness and Reliability are a function of time, whereby the "time" is measured differently
  - Operating time
  - Mileage (automotive)
  - Durability
  - Load cycles
- Not directly measureable
- Described by survival probability



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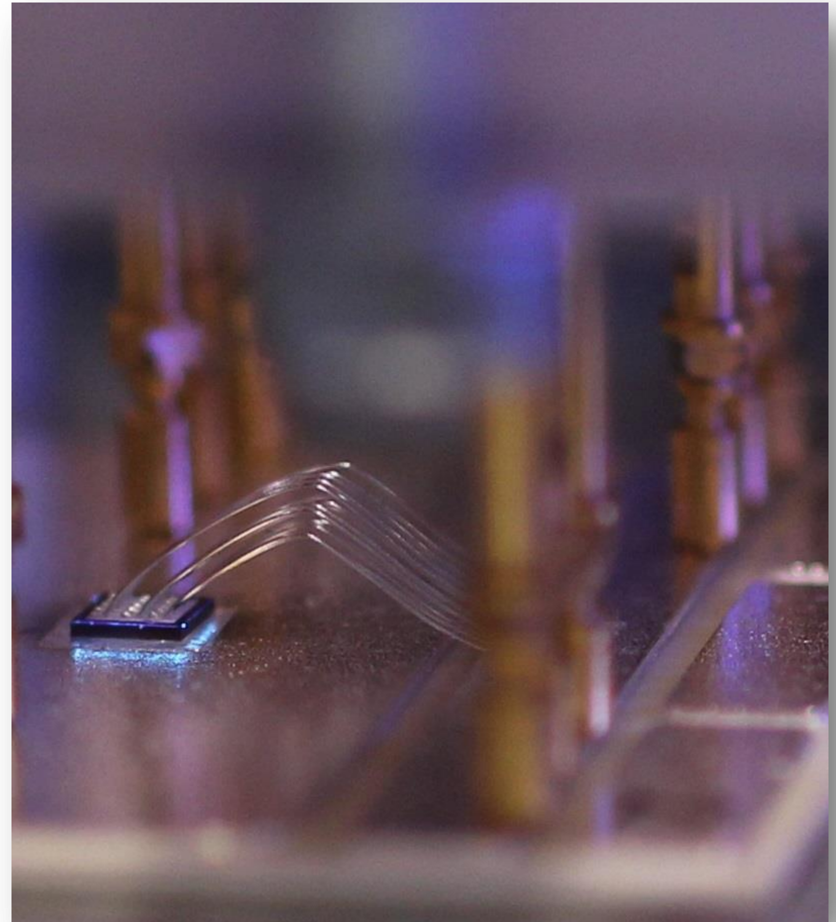
Reliability Testing

- Lifetime is tested by (accelerated) lifetime tests
  - Acceleration is made by overload
  - Important: Failure mechanism must not be changed by the overload testing
- Reliability is the statistical lifetime
- Robustness compares the reliability to the mission profile and defines a robustness margin



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Reliability and Lifetime of Wide Bandgap technology

- Low $R_{DS,ON}$ or low chip size, high current density
- High switching speed, availability of high voltage unipolar devices
- High switching frequency → stress for passive components
- (High temperature operation)

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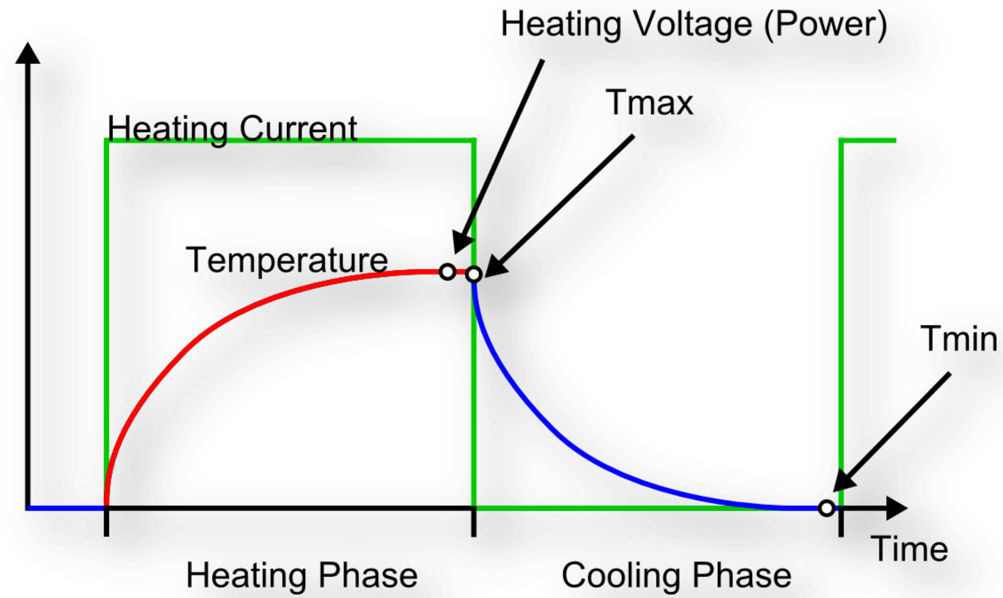
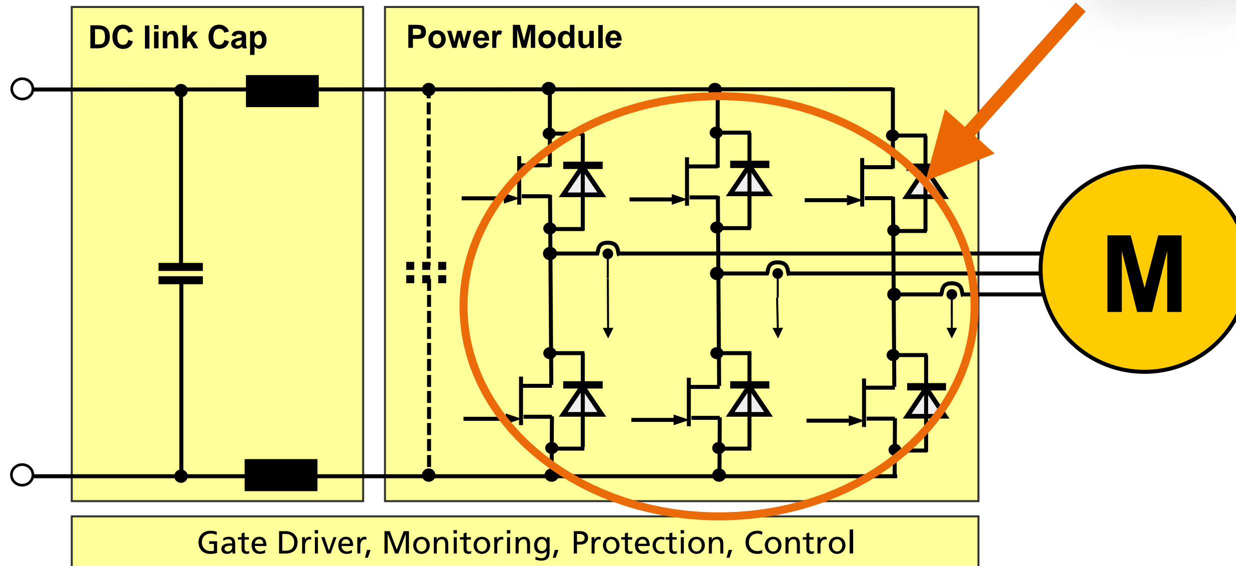
Testing Thermo-mechanical Lifetime (Power Cycling)…

- Semiconductors
  - Conduction losses
  - Switching losses





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Test at Acceleration Limit

- Static Losses of FETs
  - Heating is done by DC current (state of the art)
  - $P = I^2 * R_{DS,ON}$
  - Extremely low $R_{DS,ON}$ limits the power losses
  - dT is hard to achieve by heating current only current; may be limited by package or semiconductor die
  - Gate voltage has to be reduced down to the limits (has to be well above threshold under all circumstances)
- Solution
  - Use body diode for heating (approx. 3V forward voltage)
  - Use switching losses as additional heat source → complicated setup

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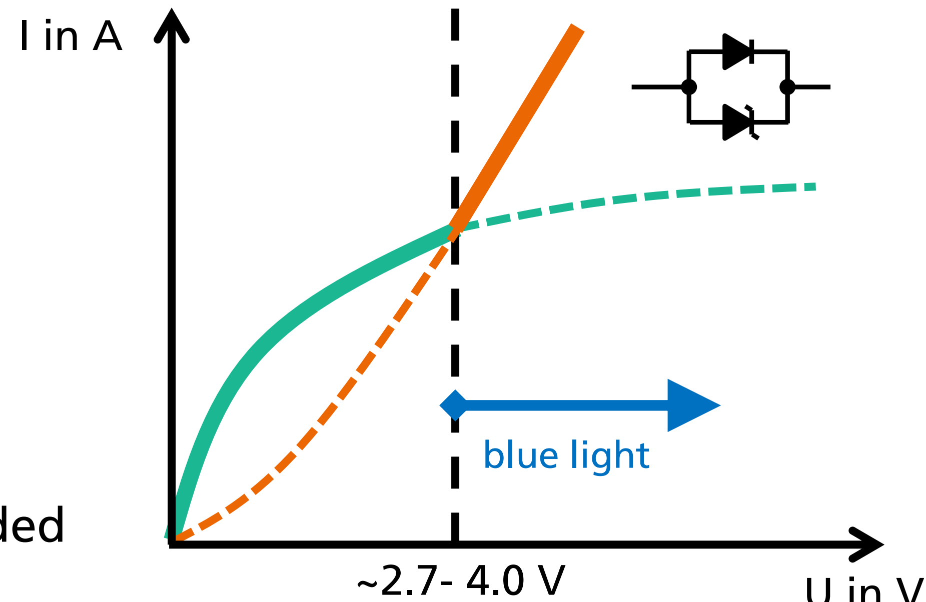
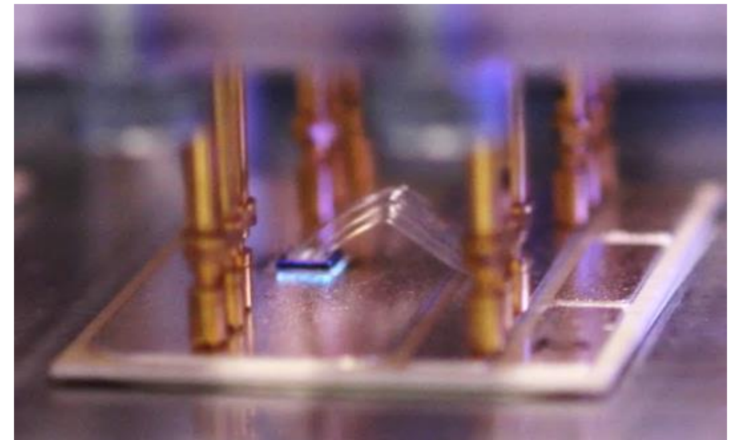
Test at Acceleration Limit



- Electric performance of the semiconductor devices under test
- Example
  - Small device → excellent heat spreading → high power loss needed
  - High heating current needed
  - SiC schottky used
  - Device operating the merged pn structure (overcurrent protection)
  - Exceeding datasheet values …



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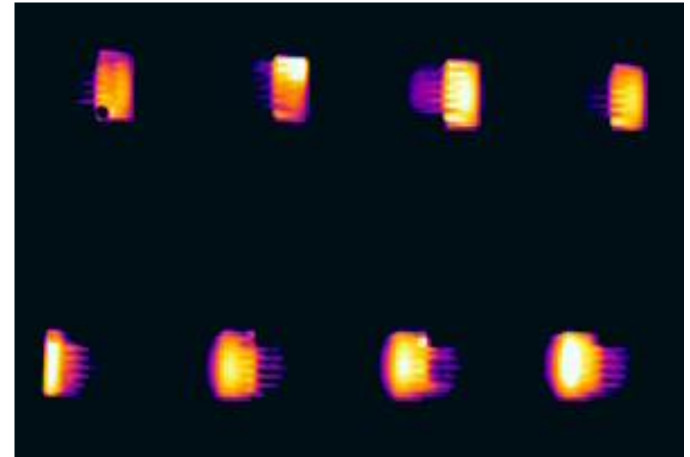
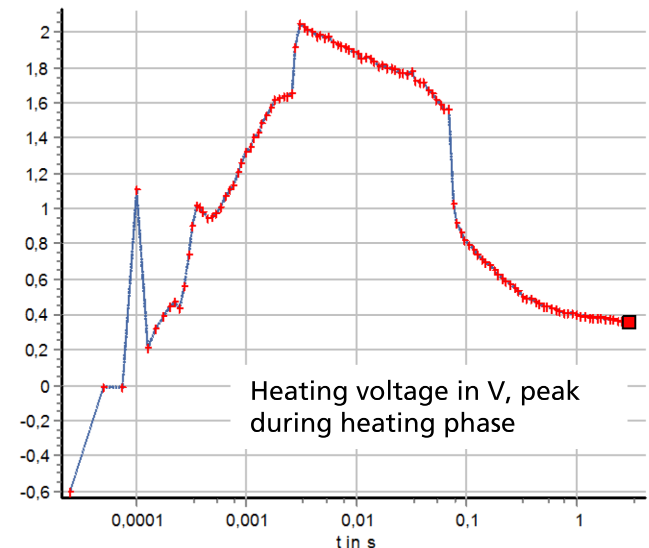
A.Hutzler et.al., Increasing the lifetime of electronic packaging by higher temperatures: solders vs. silver sintering, 64th Electronic Components and Technology Conference, ECTC 2014 : 27-30 May 2014, Orlando, Florida, USA

Test at Acceleration Limit



- For FETs: Use low gate voltage
  - Higher forward voltage, lower current, higher losses → higher temperature swing
- Drawback
  - Negative temperature coefficient of threshold voltage
  - Different heating of semiconductors according to they local electrical and thermal performance
  - No application relevant situation
  - Virtual temperature measurement becomes free to interpret
  - Inhomogeneous temperature distribution over chip surface
  - Possible overheating in the first ms



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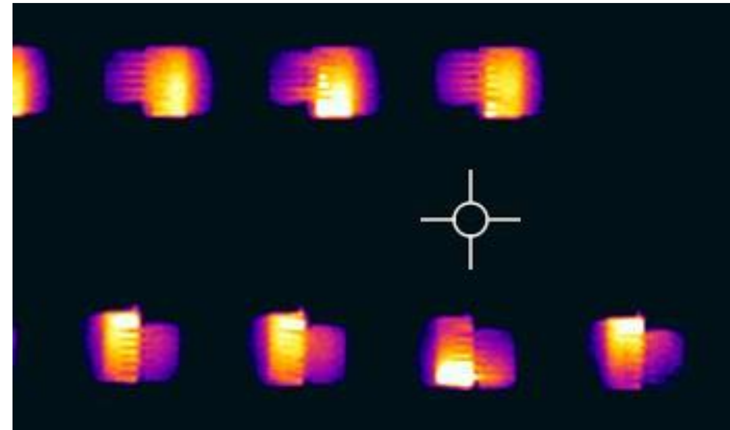
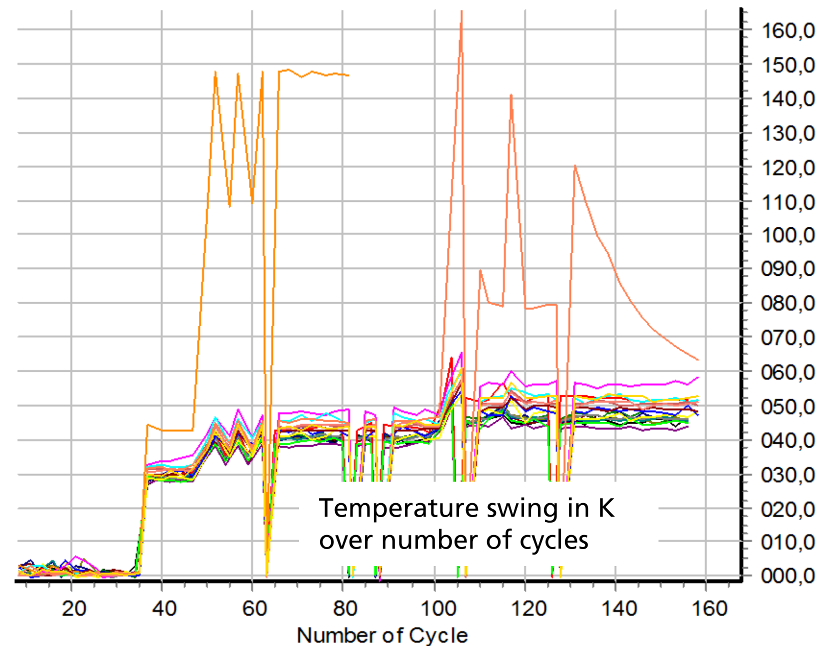
Test at Acceleration Limit



- For FETs: Use body diode for heating
  - Higher forward voltage, lower current, higher losses → higher temperature swing
- Drawback
  - Negative temperature coefficient
  - Different heating of semiconductors according to they local electrical and thermal performance
  - No application relevant situation
  - Virtual temperature measurement becomes free to interpret
  - No control – no fine tuning
  - Inhomogeneous temperature distribution over chip surface



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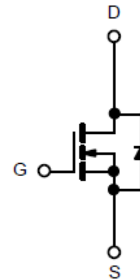
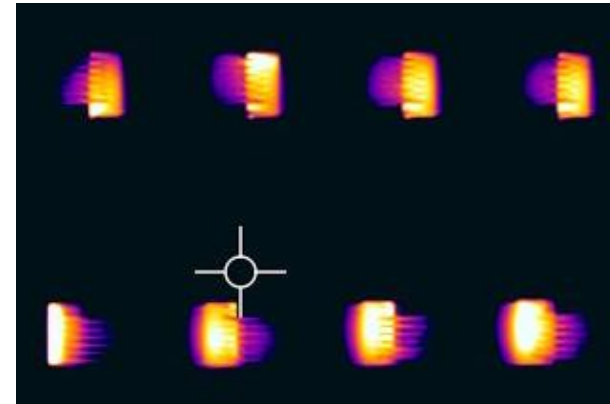
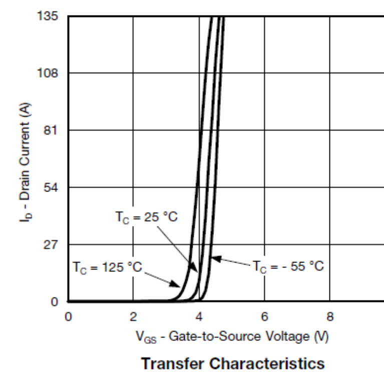
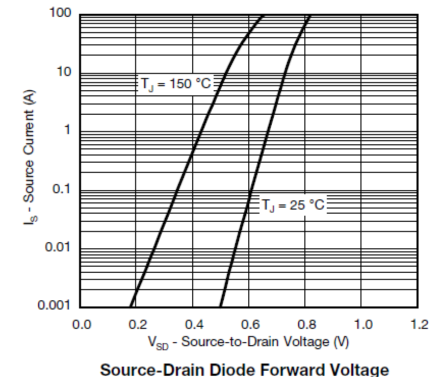
Test at Acceleration Limit

- Work around #1 (for FETs only):
- Use body diode for heating and slightly open FET channel at the same time
  - During the heating up: application of a positive gate voltage near the threshold
  - Temperature difference between chip is much better
  - More homogeneous temperature distribution on chip
- Operating principle
  - PN diode is in parallel to the FET
  - FET's threshold decreases with increasing temperature → channel opens at hot regions, cutting down temperature self-controlled
  - But: 2. theoretical possibility: dominant heating current flows through FET channel intensifying the hot spot
  - Behavior dependent on electro-/ thermal performance of the semiconductor
- Drawback: No common mind, no standard









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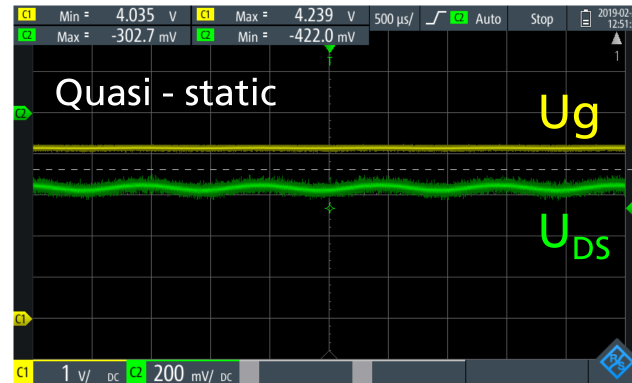
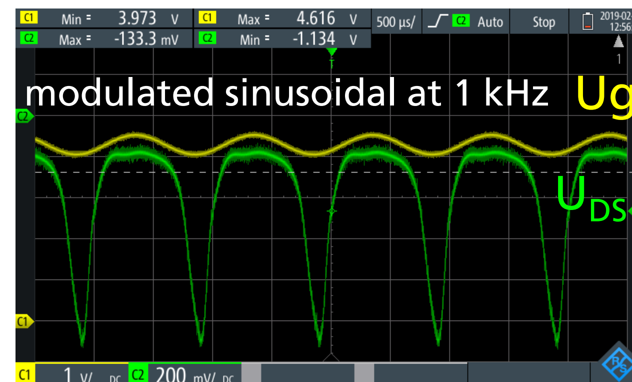
Test at Acceleration Limit

- Work around #2 (for FETs only):
- Operating principle
  - Simple applied "Switching losses"
  - Heating in forward direction
  - gate voltage with AC (any waveform) plus DC offset
  - Heating power is equivalent to the area below U_{DS} curve
  - Very stable operating point
  - No inhomogeneous chip temperature
- Drawback:
  No common mind, no standard





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Drift of FET's Gate Threshold Voltage

- Drift of gate threshold voltage
  - Heating power @ static gate voltage changes due to the effect
  - Dependent on test parameters
    - t_{on} t_{off} ratio
    - Temperature
    - Voltage levels for heating and cooling
    - Maybe pos./ neg. gate voltage impact different
    - Reversible, particular during test system shut down (undefined down time)
- Solution
  - Identify drift and re-adjust gate voltage during test
  - Develop new end of life failure criterion

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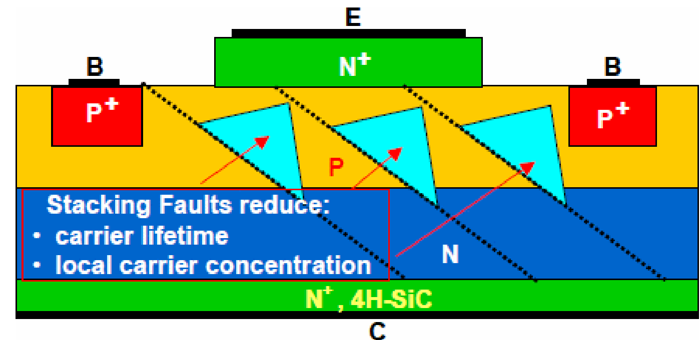
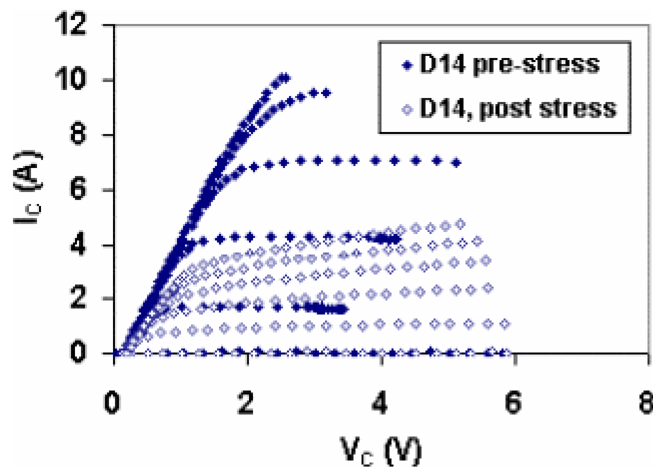
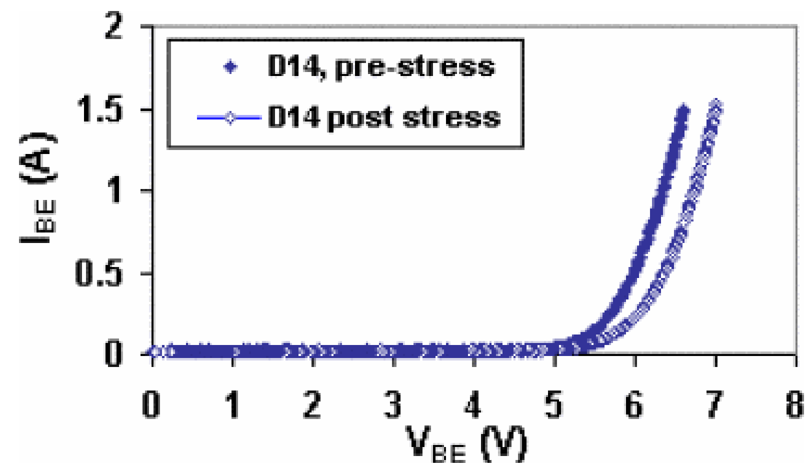
SiC Bipolar Degradation

- SiC MOSFETs have **bipolar** body diodes
- SiC bipolar devices suffer from material defects
- Failure cause: Current and temperature







Qingchun (Jon) Zhang et.al.: Degradation Mechanisms in SiC Bipolar Junction Transistors

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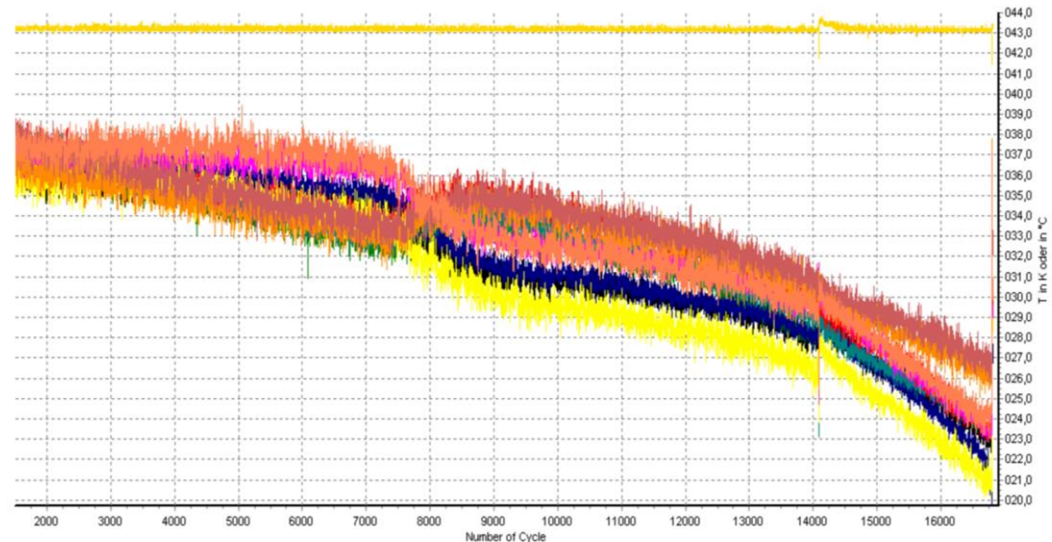
SiC Bipolar Semiconductor Parameter Drift

- SiC body diode my suffer from degradation (some manufacturers use a pre-scanning of wafers to sort out infected areas)
- Problem
  - Temperature sensor is drifting away
  - Poor results by indirect temperature measurement
- Solution
  - Recalculate temperature by voltage offset (error prone)
  - Recalibration of sensor voltage
  - Develop new end of life failure criterion
  - Just wait (seems to be a solved issue because of improved wafer quality)



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WBG Semiconductors Challenges Summary

- Big variety of challenges
- The test acceleration limit is a general problem for WBG
- The drift of the semiconductor parameters cause poor accuracy of the indirect temperature measurement
  - Solutions are available
  - No common understanding for testing of WBG devices at the acceleration limit
  - Good news:
    The aging of semiconductors is an additional test result which is gained free of charge!
    → why not use it and define new EOL criteria

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Power Cycling Lifetime - SiC

	Si @ 20°C	SiC-4H 20°C	Lifetime compared to Si
Thermal conductivity in W/(m*K)	150	380	☹ Chip have higher temperature due to better heat spreading[1]
Specific heat capacity in J/kg*K	700	690	😐 Not a big difference
CTE in ppm/K	3	4,3	☺ Better „matching" to packaging materials
Youngs Modulus in GPa	162	507/547/ 159/108 (anisotropic)	☹ Increased stress
Die thickness in µm for 650V	40...120	180…325 +/-40µm	☹ Increased stress ☹ Wider distribution
Normalized die size in mΩcm² @ 25°C	142mm²*11mΩ = 15,6 [3]	26mm²*25mΩ = 6,5 [2]	☺ or ☹ 2,4x smaller die size
Normalized die size in mΩcm² @ 150°C	142mm²*14mΩ = 19,9 [3]	26mm²*25mΩ = 11,1 [2]	☺ or ☹ 1,8x smaller die size

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[1] Ch. Herold et.al.: Power cycling capability of Modules with SiC-Diodes, CIPS 2014, February, 25 – 27, 2014, Nuremberg/Germany
[2] Wolfspeed CPM2-1200-0025B
[3] Infineon IGC142T120T8RH

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Power Cycling Lifetime - SiC

- Lifetime of SiC is about 30%..40%[1] than of Si (Sn solder, Al bond wires)
- Application
  - Temperature swing has to be lower in order to fulfill lifetime requirements
  - Bigger chip size is needed
- Outlook to the future
  - $R_{DS,ON}$ reduction will go on
  - Improvement is based on technology improvements and back grinding of SiC-Wafers
  - Dies will be less thick → thermo-mechanical lifetime will increase
  - At the same time the current density will increase → smaller die

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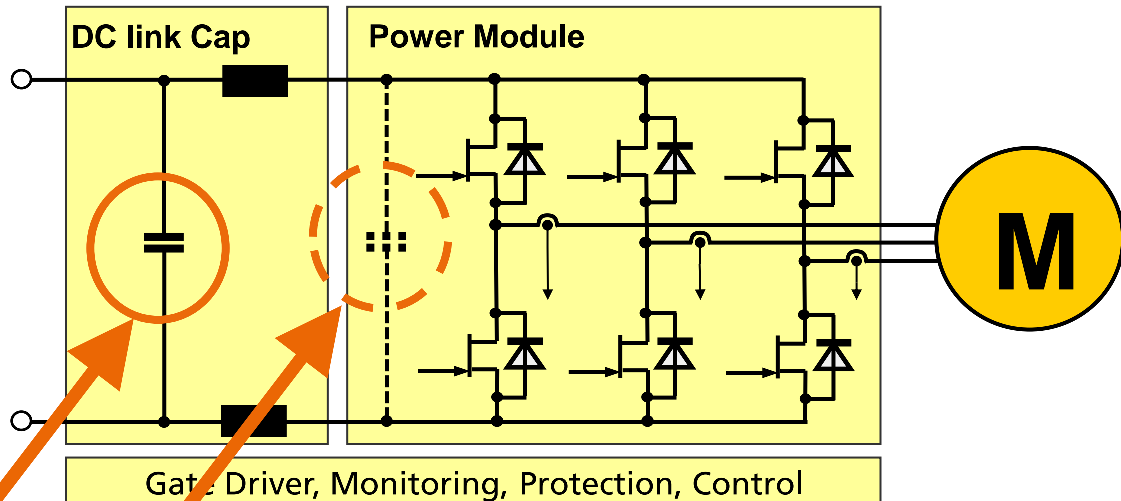
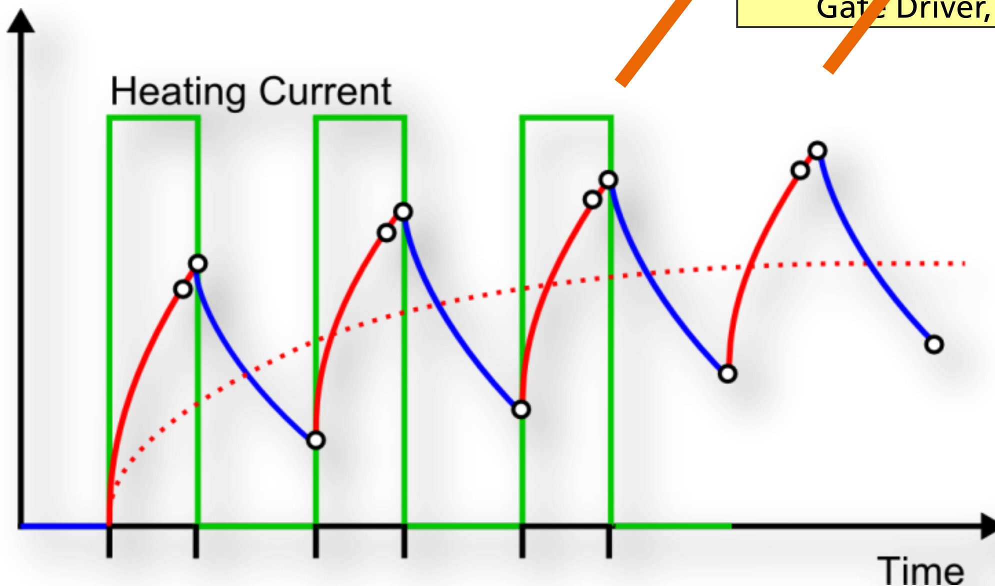
[1] Ch. Herold et.al.: Power cycling capability of Modules with SiC-Diodes, CIPS 2014, February, 25 – 27, 2014, Nuremberg/Germany

Testing...

- Capacitors
  - 6th current harmonics
  - Commutation energy
  - EMI filtering
  - (Load shedding)





- Capacitors can have significant self heating
  - Ohmic losses by load current
  - Dielectric losses by voltage ripple and frequency

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Capacitors for power electronics

- Applications
  - DC-Link
  - Snubber
- Technologies
  - Film
  - Electrolytic
  - Ceramic
  - Silicon

RONG Rui , „AN-Power stage of 48V BSG inverter Reference design with TOLL & TOLG MOSFET“, www.infineon.com, 2018

Maximum efficiency for inverters
Reference design, TDK Electronics AG, 2017

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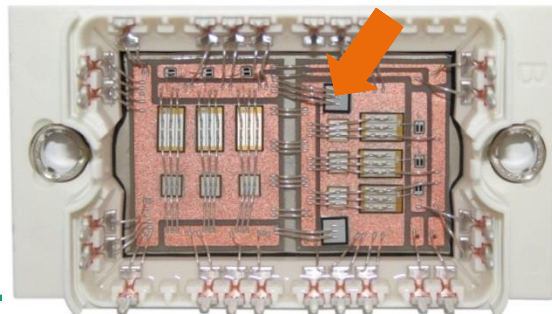

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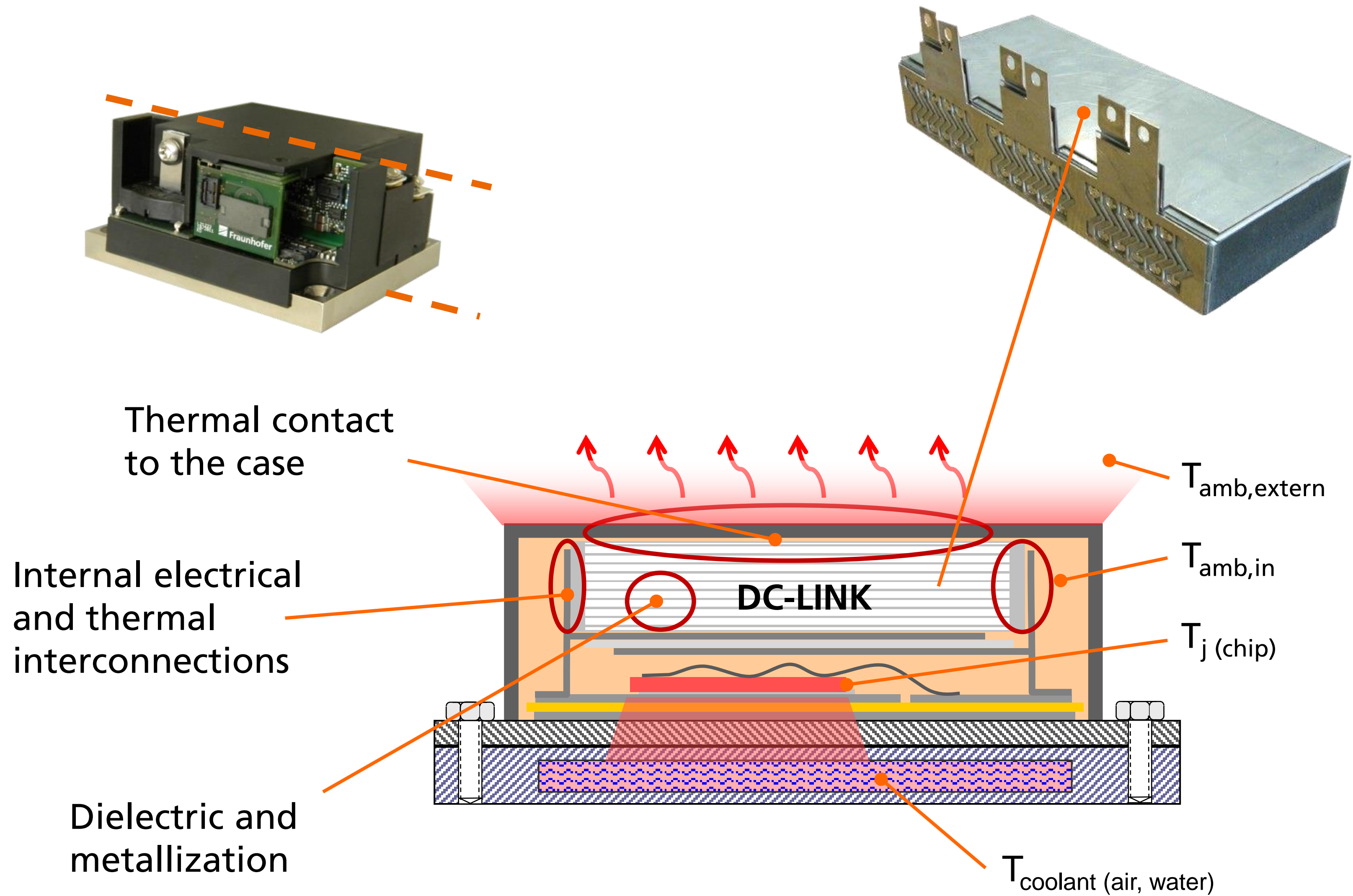
Worth to test



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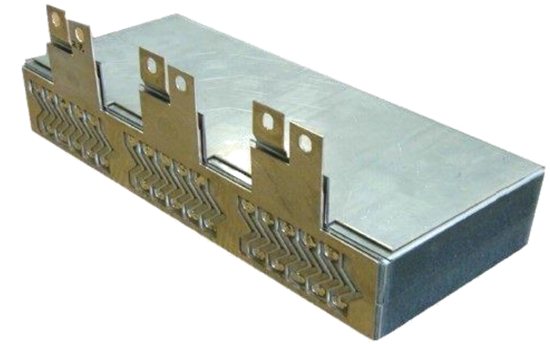
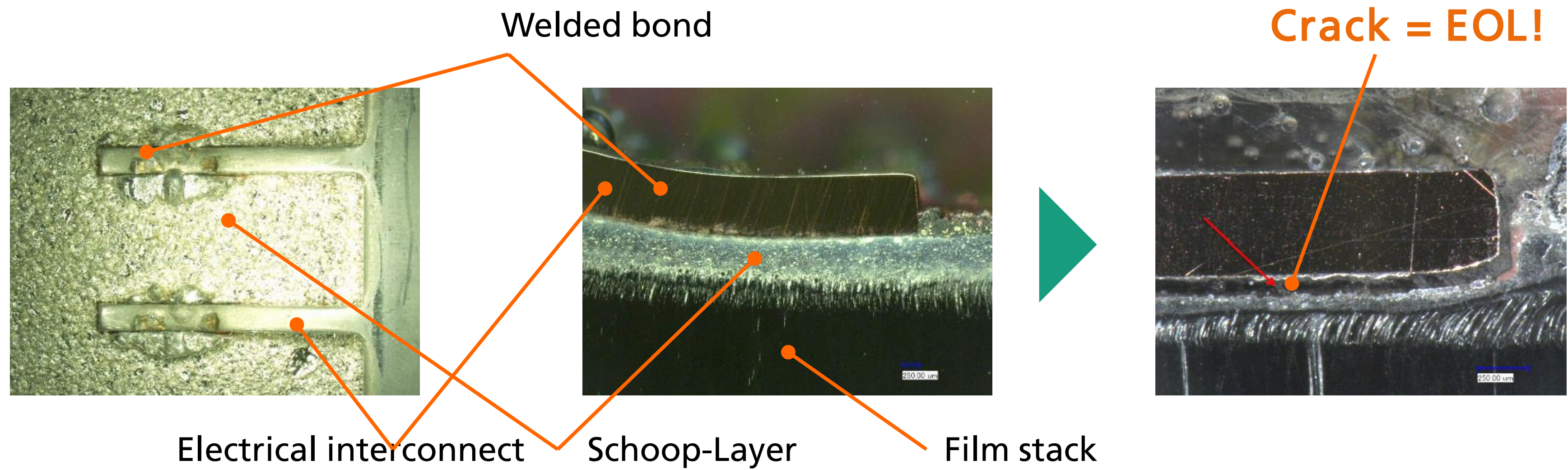
Example: Film Capacitor



- Test with application near self heating
- Materials have different mechanical properties
  - Coefficient of thermal expansion (CTE)
    - PP: 100ppm/K; Zn: 30ppm/K; Cu: 17ppm/K
  - Young’s Modulus, fracture toughness, … (all temperature dependent)
- Result: Thermo-mechanic ageing



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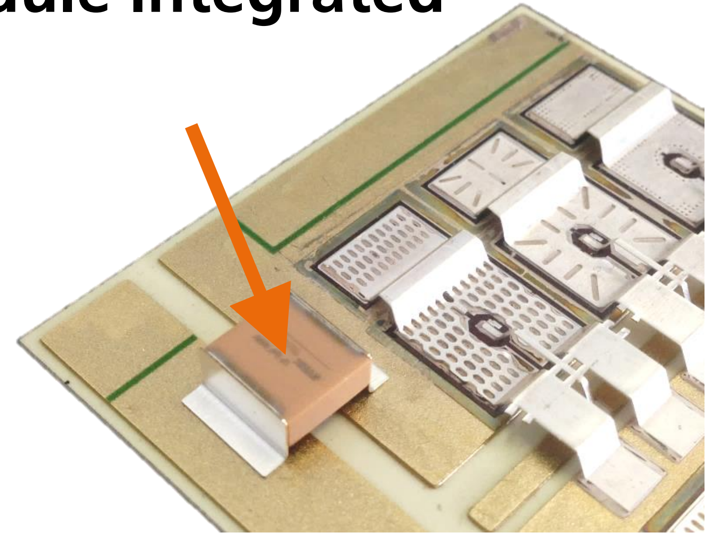
Example: Ceramic Capacitor – Module Integrated

- Test with application near self heating
- “Commutation capacitor” to reduce the parasitic inductance of the commutation cell in snubber or dc-link configuration
- Ceramic capacitors have no ductile materials (capacitor crack is a well known failure mechanism)
- Capacitors can have significant heating
  - passively by the power semiconductor → active PCT of active devices
  - active by own power losses → active PCT of passive devices



Ceramic DC link capacitor at end of life

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Capacitors summary

- Current test for (power)capacitors: AEC-Q200/ JEDEC
  - Standards made for small signal components, mainly SMD on PCB
  - Based on constant failure rate
  - Passive temperature shock test used
  - No application near (inhomogenious) temperature distribution
  - Robustnesss margin unknown (qualification, no EOL testing)
- 1. step to improve standardisation for testing of DC link film capacitors „Qualifikation von Zwischenkreis-kondensatoren für den Einsatz in Komponenten von Kraftfahrzeugen, ZVEI“, 2017
- No data basis for thermo-mechanic wear out failures for power capacitors available → reduction of over engineering not possible
- Outlook: Testing with application near temperature distribution (=self heating) to EOL
  - Determination of failure mechanisms
  - Identification of weak points
  - Development of systematic technology improvements
  - Definition of end of life criteria
  - Life time modelling, based on physics of failure

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Summary

- Wide band gap (SiC presented) has some issues not known from Si
  - Parameter drift
  - Problematic thermo-mechanical testability due to extremely low $R_{DS,ON}$
  - Overall power cycling lifetime is 30% of Si caused by material and device thickness
  - Power cycling testing shows most of the mechanisms for free !
- Fast switching moves passives into the focus
  - Capacitors get significant self heating
  - Especially power module integrated snubbers may have high power losses
  - Cyclic self heating degrades interfaces and dielectric
  - No data basis and models available → a lot of research work to do

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