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Reducing On-Resistance for SiC Diodes by Thin Wafer and Laser Anneal Technology

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Motivation

- Minimizing power losses by thin wafer and laser anneal technology
- SiC substrate thickness usually 350 µm, having a relatively high contribution to the total on-resistance R_{ON} with no electrical advantage for the device [1]
- Device performance benefits from a thinner SiC substrate thickness: noticeable reduced on-state forward voltage drop V_F while maintaining blocking capabilities
- Reducing wafer thickness to the largest possible extent without compromising wafer manufacturability and device functionality

Device fabrication

- 6 A 650 V SiC Merged-pin-Schottky (MPS) diodes designed and fabricated by Fraunhofer IISB on commercial 100 mm epitaxial wafers
- Al-implantation and high temperature annealing for JBS patterning
- Silicided Ti (TiSiC) as ohmic contact on p^+ for conductivity modulation
- Wafer grinding to a final thickness of approx. 90 µm with 65 µm SiC substrate and 25 µm consisting of epitaxial layer, power metallization and polyimide passivation
- Backside ohmic contact formation via laser annealing of sputtered Ni

Wafer Thinning

- Temporary bond to a glass carrier substrate for mechanical stabilization
- Wafer frontside spin coated with a specific thermoplastic adhesive film, highly suitable to level 3D structures like thick metal and polyimide passivation layers
- Due to increased risk of wafer breakage wafer thinning is applied at the end of the process chain on front side finished devices

Laser Annealing

- Conventional annealing not applicable due to temperature sensitive wafer front side
- Minimizing thermal impact on finished front side by backside laser annealing
- Homogeneous silicidation across the wafer surface due to scan patterning process with defined laser beam energies
- Significant benefits on the uniformity of the backside ohmic contact resistance

Substrate Characterization

- Fig. 1: Facet occurrence during sublimation growth of SiC: enhanced impurity and dopant incorporation [2]
- Wafer opacity increases with higher doping density

Fig. 1: UV-PL image of epitaxial wafer with observable facet region on the right wafer side

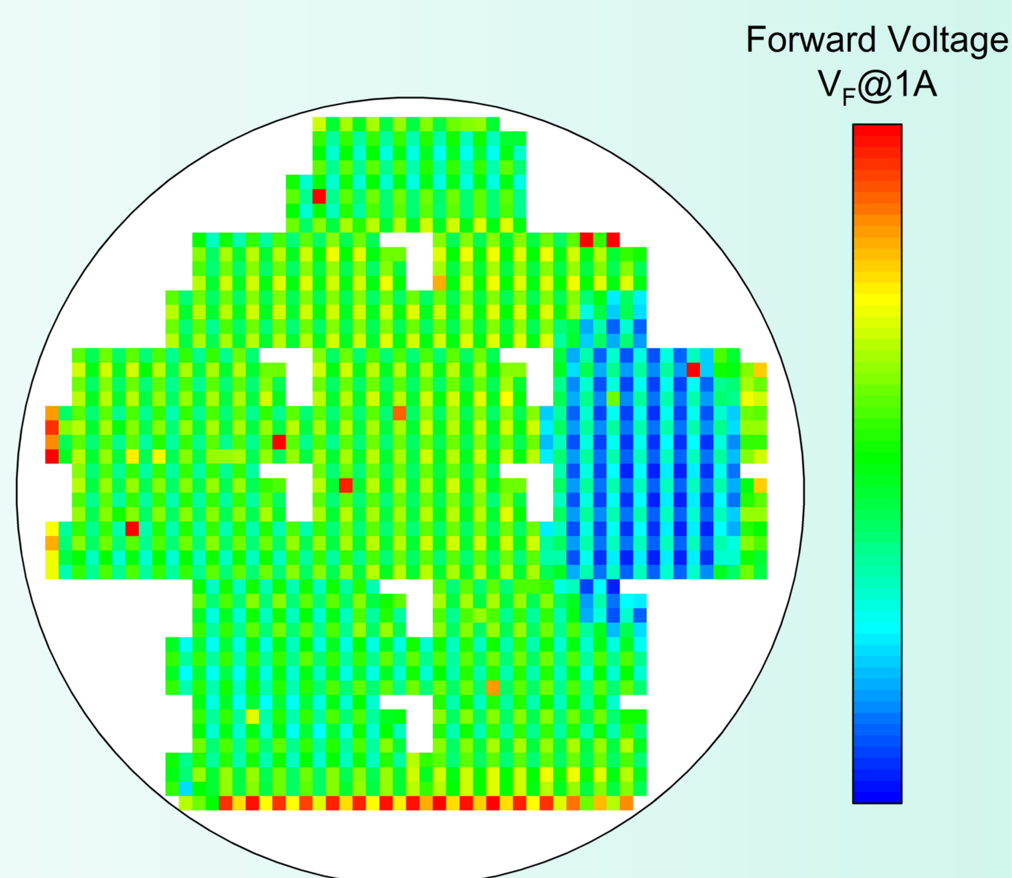

Fig. 2: Heatmap showing forward voltage distribution at 1A (lower V_F represented by more blueish color, checker-board pattern due to 2x2 design array arrangement)

Electrical Characterization

- Fig. 2: Accumulation of devices with lower forward voltage at 1 A within the facet region ($\Delta V_F \approx 4$ %)
- Fig. 3: Significantly tightened forward voltage distribution for thinned devices ($\Delta V_{F,\ Thinned} \approx 9$ % vs. $\Delta V_{F,\ Initial} \approx 15$ %)
- Reducing R_{ON} by approx. 30 % to 90 mΩ and 60 % to 12 mΩ in Schottky and conductivity modulation state, resp.
- Fig. 4: Clear dependency between facet region and device on-resistance
- Fig: 5: Maintaining blocking capabilities of more than 1 kV with leakage currents less than 1 µA at 650 V
- Fig. 6: No direct correlation of breakdown capability with substrate thickness or doping concentration ($\Delta V_B \approx 1$ %)

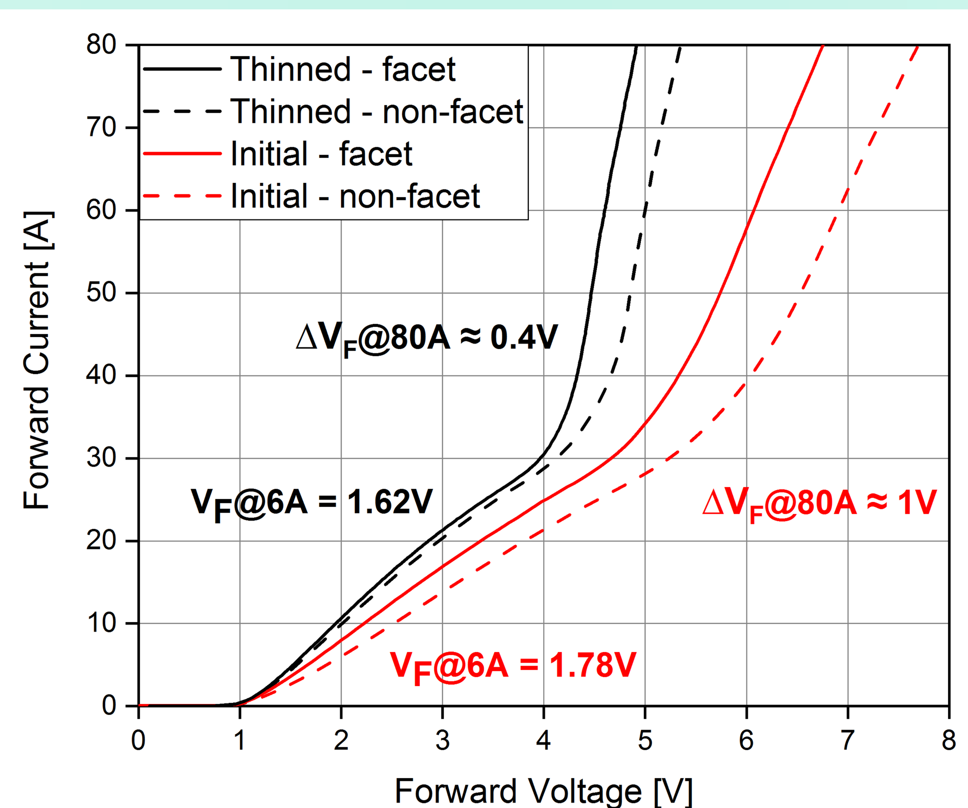

Fig. 3: Forward characteristics of similar devices, located on facet and non-facet region, before and after thinning

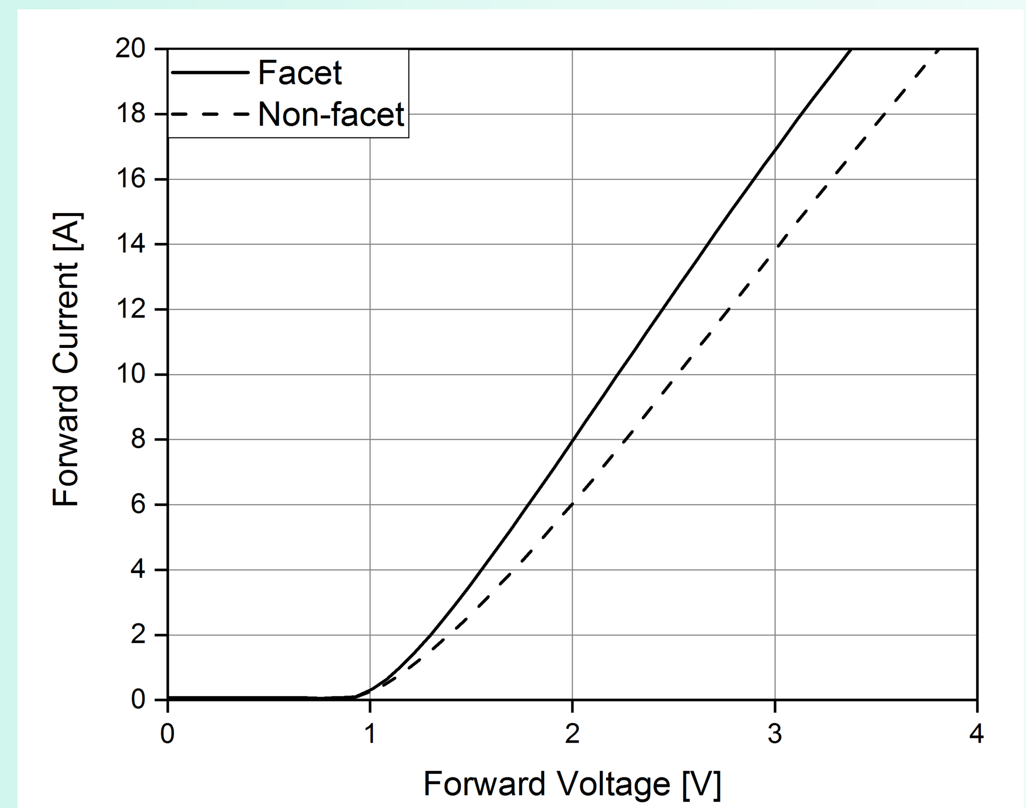

Fig. 4: Zoom-in in forward characteristics of similar devices, located on facet and non-facet region

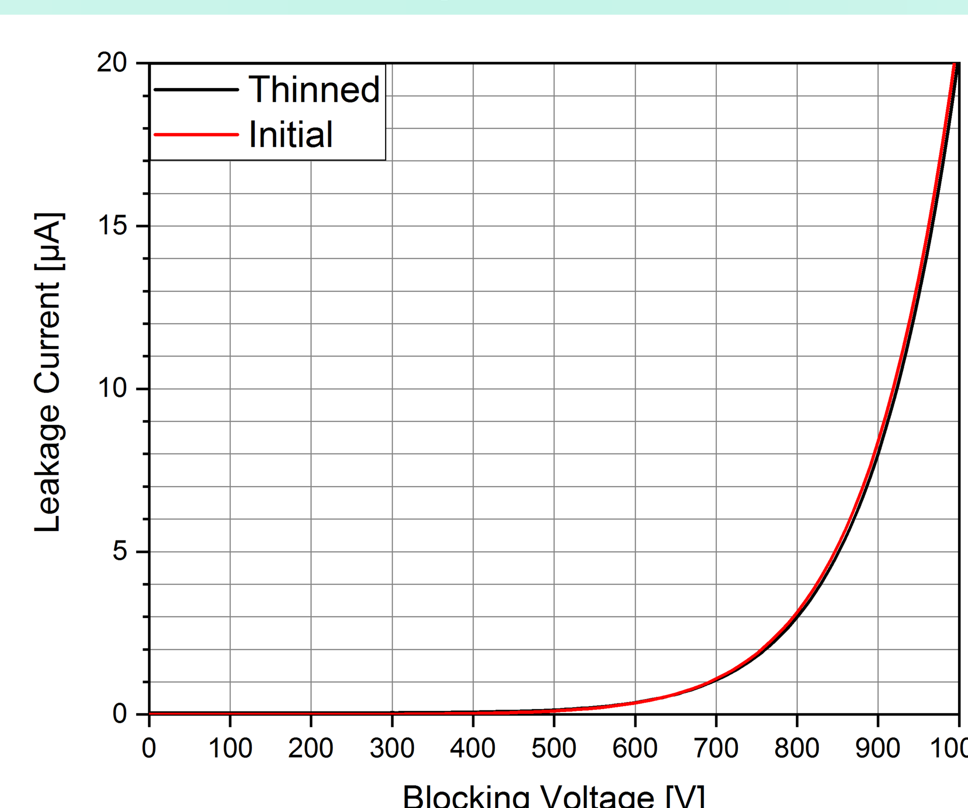

Fig. 5: Reverse characteristics of similar devices, before and after thinning

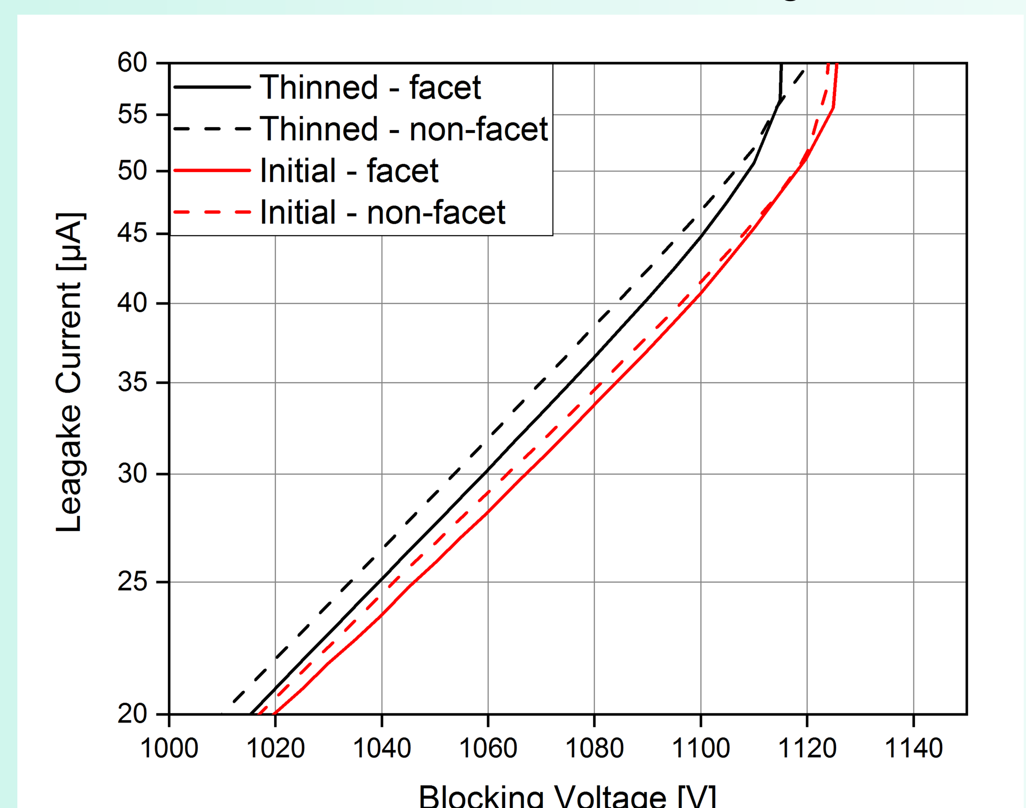

Fig. 6: Reverse characteristics of similar devices, located on facet and non-facet region, before and after thinning

Acknowledgements

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Summary

- Successful integration of wafer thinning and laser annealing to 6 A 650 V SiC MPS fabrication process at IISB
- Significant forward voltage drop VF reduction with no downsides in terms of blocking capability
- Lowering on-resistance variation due to facet occurrence by reducing substrate thickness
- Tightening of voltage drop distribution across the wafer by reduction of substrate doping concentration variations

References

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