A 10.5 µW programmable SAR ADC Frontend with SC Preamplifier for Low-Power IoT Sensor Nodes

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Abstract—Massive deployment of wireless autonomous sensor nodes requires their lifetime extension and cost reduction. The analog frontend (AFE) plays a key role in this context. This paper presents a successive approximation register analog-to-digital converter (SAR ADC) with a switched-capacitor programmable gain switched preamplifier (SC PGSA), as a basic component of an integrated ultra-low power AFE. AFE resolution, sample rate and signal gain are configurable between 6 to 13 bit, 1 to 10 kS/s and -6 to 12 dB, respectively. The circuit draws 10.5 µW from a 1.8 V standard supply voltage, achieving an effective number of bits of 12.6 bit and a Walden figure of merit of 169.1 fJ/st. and 30.6 fJ/st., computed with and without preamplifier, respectively. The circuit is employed in a modular internet of things sensor node, suitable to be solely powered from microenergy sources (energy harvesters). In order to feed charge-scaling SAR ADC inputs with the sensor voltages, typically a preamplifier stage is implemented, which can create energy overhead of magnitudes larger than the ADC power. This paper presents a duty-cycled preamplifier with programmable gain for SAR ADCs, utilizing switched-capacitor switched-opamp technique in the SC PGSA. No additional buffer circuitry is needed to charge the SAR ADC, and the preamplifier design is relaxed in power constraint. The circuit targets the low-cost internet of things market. Cost efficiency is achieved by technology choice, wide configurability and shortened ASIC design cycles. The latter results from partly generated layout, easing reuse of circuit parts from a different CMOS node. A testchip in a low-cost 180 nm silicon-on-insulator technology was fabricated.

Index Terms—SAR ADC, analog frontend, ultra-low power, harvester-powered autonomous sensor node

I. INTRODUCTION

Wireless autonomous sensor nodes (SNs) are basic hardware components of the internet of things (IoT), serving the digital transformation of production, mobility and housing. Large-scale automation requires wireless sensor networks with low costs of purchase, installation and maintenance. Thus, SNs with life spans of more than ten years are profitable. The connection of SNs to a power supply is often not feasible, cost-effective or desired in existing substrate. The nodes must be powered by a local source. Recent surveys show battery- and harvester-powered SNs to be restricted to few micro-watts in power consumption to achieve long life cycles ([1], [2]). Even battery usage can be undesired due to poisonous, rare or problematic materials. Moving from ultra-low power (ULP) towards Zero-Power IoT hardware [3], which is powered from renewable scavenged energy, the power consumption of each and every component must be reduced dramatically.

While SNs integrate several functional blocks like microprocessor, memory, power management, clock management, transceiver, etc. [4], particular interest has been spent on the analog frontend (AFE). The charge-redistribution successive approximation register analog-to-digital converter (SAR ADC) is an optimal candidate to achieve low-to-medium resolutions and sample rates, and scalability across different CMOS nodes ([5], [6]). However, previous works tend to exclude the problem of charging the dynamically changing capacitive load of a SAR ADC, which is particularly focused in this work.

This paper presents a configurable 6 to 13 bit, 1 to 10 kS/s SAR ADC with a switched-capacitor programmable gain switched preamplifier (SC PGSA), utilized in an ULP AFE. The SAR ADC is flexible in parameters and hardware, in order to maximize reusability. With Intelligent IP (IIP) methodology [7], parts of an existing design were ported from 22 nm to 180 nm SOI technology [8]. Switched-opamp (SOA) technique is utilized in the preamplifier to reduce average power dissipation down to 10.5 µW in post-layout simulations. In order to interface typical commercial sensor output voltages, a minimum voltage of 1.8 V was chosen. Therefore, the SC PGSA supports discrete gain levels of {−6, 0, 6, 12} dB and quasi-rail-to-rail input dynamic range. A test chip was fabricated in a standard 180 nm silicon-on-insulator (SOI) technology, which was chosen to enable low-cost circuit production. The simulation results were reproduced in laboratory experiments with good accuracy.

A brief overview of design limitations and the state-of-the-art is given in Section II. Section III deals with the design of the proposed AFE architecture. In Section IV, simulation results and testchip measurement is discussed. Conclusions are drawn in Section V.

II. DESIGN LIMITATIONS

Figure 1 shows a classical block diagram of an ULP single-channel AFE, consisting of track & hold (T&H) stage, continuous-time preamplifier, preliminary buffers and a SAR ADC. Numerous publications utilize the charge-scaling SAR ADC to match low-power and low-frequency requirements. As typical for digital circuits, reduction of the sample rate scales
the activity and hence the power dissipation, only limited by leakage effects. In low-frequency systems, the capacitor digital-to-analog converter (CDAC) dominates power dissipation. A vast number of CDAC switching schemes has been proposed and astounding results could be shown [9].

However, although the power dissipation of SAR ADC components can be optimized over wide ranges, the energy demand of the total AFE might not benefit dramatically. One reason is the transfer of the unbuffered sensor output voltages via low-noise preamplifier to the capacitive input of the SAR ADC. This power-demanding analog operation and its effect to the overall AFE power consumption is covered only by few publications. As shown in Figure 1, the input of the SAR ADC forms a switched-capacitor (SC) load, functioning as a T&H stage, and can reach for typical unit capacitors (around 10 fF to 50 fF) and typical resolutions (around 8 bit to 12 bit) the range of few picofarads. In order to decouple the sensible output node of the preamplifier from this switched load, analog buffers can be used [6]. However, the limitations of this approach are obvious. Consider a common NMOS intrinsic gain stage, as shown in Figure 1, which can be found in the output stage of a typical operational transconductance amplifier (OTA). The charging speed of the capacitive load is determined by slew rate (SR):

\[ \text{SR} = \frac{I_{\text{out}}}{C_{\text{DAC}}} \]  

where \( I_{\text{out}} \) is the OTA output current and \( C_{\text{DAC}} \) is the SAR ADC total input capacitance, dominated by the CDAC. If the OTA bandwidth is very high compared to the ADC clock frequency \( f_{\text{clk}} \), the minimum SR is determined by the minimal allowed slewing time, which is a fraction of the sampling phase pulse width \( t_s \), and the maximum possible voltage step at the ADC input, which equals its full-scale range \( V_{\text{FSR,ADC}} \):

\[ \frac{I_{\text{out}}}{C_{\text{DAC}}} \geq \frac{V_{\text{FSR,ADC}}}{t_s/k} = V_{\text{FSR,ADC}} \cdot f_{\text{clk}} \cdot k \]  

Typically, one ADC clock period \( t_{\text{clk}} = 1/f_{\text{clk}} \) is spent for the sampling phase, while each step of the bit conversion phase takes one cycle as well, i.e., \( t_s = t_{\text{clk}} \). Considering a full-scale range of 1.7 V, a clock frequency of 140 kHz, \( k = 3 \), and a \( C_{\text{DAC}} \) of 6.5 pF, \( I_{\text{out}} \) equals 4.6 \( \mu \)A. The DC power consumption for a supply voltage of 1.8 V equals around 8.3 \( \mu \)W per current branch, which becomes clearly a dominating factor, if two to three current branches need to be considered for a standard OTA.

Two methods to relax the pramplifier speed specification are the extension of sampling phase ([5], [10]), and the use of a parallel charge reservoir. Both methods affect power consumption and sample rate of the system. Therefore, the switched operation of a SOA as preamplifier is proposed in this work, changing continuous-time to sampled circuit operation.

III. CHANNEL ARCHITECTURE

The architecture of the proposed ULP AFE is depicted in Figure 2. The SC PGSA, which serves as programmable gain preamplifier with integrated T&H stage, is directly connected to the SAR ADC, additional buffers are omitted. The digital ADC inputs are \( D_{\text{clk}} \) (clock) and \( D_{\text{soc}} \) (start-of-conversion); the digital outputs are \( D_{\text{out}} \) (data-out), \( D_{\text{soc}} \) (end-of-conversion), and three non-overlapping clock signals \( \phi_0 \), \( \phi_0' \), and \( \phi_1 \).

The specifications of the AFE were set to match application as part of a modular IoT environmental sensing node. Medium resolution up to 13 bit and medium sample rate up to 10 ks/s are chosen to enable classification of typical environmental signal types. After surveying the market of commercially available sensor parts, a quasi-rail-to-rail input voltage range of 1.8 V was specified. This eases the modular interconnection of a wide range of available sensor components and enable classical design approaches. While digital circuitry does not benefit from higher \( V_{\text{DD}} \) in particular, analog circuits tend to consume less power due to higher signal-to-noise-ratios.
A. SC Programmable Gain Switched Preamplifier

The SC PGSA (grey-boxed in Figure 2) was explored in [11] and consists of a SOA, CMOS switches, feedback capacitor \(C_{fb}\) and variable T&H capacitor \(C_{th}\). Figures 3a to 3c show equivalent circuit diagrams in phases \(\phi_1\), \(\phi_0'\) and \(\phi_0\). In phase \(\phi_1\) (Figure 3a), \(C_{th}\) tracks the differential input voltage \(V_{in}\), while the SOA is powered down and \(C_{th}\) is shorted. Phase \(\phi_0'\) (Figure 3b), which starts slightly (one half clock cycle) before \(\phi_0\), powers up the SOA. The feedback path of the SOA remains shorted by \(\phi_1\). Phase \(\phi_0\) (Figure 3c) is the amplification phase, where voltage gain \(A_v\) is determined by (3):

\[
A_v = \frac{C_{th}}{C_{fb}} \tag{3}
\]

The clock generation is derived from ADC operation phase, as depicted in Figure 4. The SC PGSA is enabled shortly before the sampling phase, while it is powered down during bit conversion phase. The qualitative waveform of the total power dissipation \(P(t)\) is depicted in the lower half of Figure 4. The operating regime can be described as follows:

**ADC Idle/Reset:** \(\phi_1 = 1, \phi_0' = 0, \phi_0 = 0\). For \(D_{soc}\) low, PGSA and ADC are powered down and in reset phase, respectively. In this phase, no static power is dissipated, except for leakage power \(P_{dc,\text{leak}}\). Sampling capacitor \(C_{th}\) tracks the input voltage \(V_{in}\).

**PGSA Operation:** \(\phi_1 = 1, \phi_0' = 1, \phi_0 = 0\). The PGSA is powered on slightly (one half clock cycle) before ADC sampling, to ensure proper start-up. The ADC remains in reset phase. \(P(t)\) is dominated by the DC power of the PGSA, \(P_{dc,\text{PGSA}}\).

**ADC Sampling:** \(\phi_1 = 0, \phi_0' = 1, \phi_0 = 1\). The PGSA changes from sampling to amplification phase, while the ADC changes from reset phase to sampling phase. ADC sampling switches are closed and \(C_{DAC}\) is loaded with an amplified sample of \(V_{in}\). In this phase, a considerable amount of dynamic power dissipation \(P_{dyn,\text{PGSA}}\) must be accounted for charging \(C_{DAC}\) capacitors of the SAR ADC.

**ADC Conversion:** \(\phi_1 = 1, \phi_0' = 0, \phi_0 = 0\). The PGSA is powered down, and \(C_{th}\) is tracking \(V_{in}\). The ADC fulfills bit conversion operation, while its sampling switches are highohmic. In this phase, except for leakage, no static but only dynamic power \(P_{dyn,\text{ADC}}\) is dissipated.

The synchronization of amplifier operation and SAR ADC during sampling phase achieves minimal active time of the power-demanding SC PGSA, reducing average total power dissipation \(P_{av,\text{total}}\) by duty-cycling factor \(\eta\):

\[
P_{av,\text{total}} = \sum_i \frac{t_{on,i}}{t_p} \cdot P_{dyn,i} + P_{dc,\text{leak}} = \eta \cdot P_{dyn,i} + P_{dc,\text{leak}} \tag{4}
\]

A full period \(t_p\) is divided into sampling phase \((t_s)\) and bit conversion phase \((t_{bc})\):

\[
t_p = t_s + t_{bc} \tag{5}
\]

At maximum resolution, the proposed design employs \(t_p = 14 t_{clk}\), \(t_s = t_{clk}\) and \(t_{bc} = 13 t_{clk}\), which generates an \(\eta_{SC,\text{PGSA}}\) of 10.7%. The SC PGSA design benefits from the reduced power specification, because high-gain OTA circuits can be realized.

\(C_{th}\) is realized as a two-bit binary array of unit capacitor \(C_u\) (240 fF) shown in Figure 3d. The four gain steps \(0.5, 1, 2, 4\)
are selected by varying $C_{th}$ between 1 and 8 $C_n$ with configuration bits \{s_2, s_1, s_0\}, while $C_{fb}$ equals 2 $C_n$. Static $C_{fb}$ fixes the SOA unity gain bandwidth specification. The capacitor array was implemented with IIP design flow developed at Fraunhofer IIS/EAS [7]. The semi-automated layout generation with IIP generators reduces design effort and eases further migration.

A simulated transient waveform of the SC PGSA with a $\phi'_0$ duty cycle of 50\% (for demonstration purpose) is shown in Figure 5. A differential single-tone (700 mV peak-to-peak), centered at the common-mode voltage ($V_{cm}$) of 900 mV, is applied to the differential inputs ($V_{inp,n}$). For $\phi'_0, \phi_0$ both low, the SOA is powered down, and the outputs $V_{outp,n}$ are forced to $V_{cm}$. With $\phi'_0$, the SOA powers up, while the outputs remain forced to $V_{cm}$. With $\phi_0$, $V_{outp,n}$ holds a sample of the input, amplified by $A_v$.

B. Folded-Cascode Switched-Opamp

The SOA shown in Figure 6 is the active component of the SC PGSA. A fully-differential two-stage folded-cascoded OTA (\cite{12}) with additional power-down switches was utilized. An existing design was ported via IIP layout generators from a different 180 nm technology flavor, which reduced design effort. The folded-cascode stage $M_{(10-12)}$ achieves high gain bandwidth, but shows reduced output range. The voltage at nodes $V_{fb,n}$ clips around $V_{TH5} + V_D\cdot S\cdot C_{sat3}$ and $(V_{DD} - V_{TH7} - V_D\cdot S\cdot C_{sat9})$ as soon as the current mirror transistors leave saturation. $V_{TH}$ and $V_D\cdot S\cdot C_{sat}$ are threshold and saturation voltages. Since the SAR ADC has an input range close to rail-to-rail, a reduced output range of the SOA results in unused code steps and therefore reduced efficiency. The second common-source gain stage $M_{(11-14)}$ increases the range of $V_{outp,n}$ from quasi-rail-to-rail, smoothly leaving saturation around $V_{DS\cdot C_{sat13}}$, which showed efficiency for this design. The second stage adds phase shift due to the additional pole at the output nodes, which requires Miller compensation capacitors $C_{(10,13)}$ between $V_{outp,n}$ and $V_{fb,n}$. An additional compensating zero is introduced through capacitors $C_{(2,3)}$ at the cascode node [13]. The power-down mode, necessary for SOA operation, is implemented by complementary power-down switches. Bias nodes are pulled to ground or supply, disabling the current sources, to achieve close to zero leakage power consumption.

Table I shows the simulation results of stand-alone OTA with 7pF load capactitor. The circuit achieves an amplifier figure of merit (FoM\textsubscript{Amp}) of 392 MHz ∕ pF/\textsubscript{mA}, phase margin of 80°, unity gain bandwidth of 2.3 MHz and DC gain of 79.5 dB. A frequency plot of the open-loop gain is depicted in Figure 7. Within SC feedback, a minimum accuracy of 13.2 bit was simulated, being sufficient for this circuit. In the moment of start-up, the charging of bias nodes 1-4 introduces a time delay $t_{start} \geq I_{DS}V_D/C_{total}$, where $C_{total}$ is the total capacitance of each node, and $V_D$ is the diode voltage. In order to ensure fast start-up, relatively high quiescent currents of 2µA resp. 4µA were chosen for bias and core circuitry, which result in worst-corner DC power consumption of 91µW.

TABLE I: Post-layout simulation results of stand-alone folded-cascode OTA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Best Corner</th>
<th>Worst Corner</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open-loop Gain</td>
<td>86.9 dB</td>
<td>79.5 dB</td>
</tr>
<tr>
<td>Unity Gain Bandwidth</td>
<td>4.4 MHz</td>
<td>2.3 MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>84.1°</td>
<td>81.0°</td>
</tr>
<tr>
<td>DC Power</td>
<td>69.2 µW</td>
<td>91.0 µW</td>
</tr>
<tr>
<td>FoM\textsubscript{Amp}</td>
<td>392 MHz ∕ pF/\textsubscript{mA}</td>
<td>726 MHz ∕ pF/\textsubscript{mA}</td>
</tr>
</tbody>
</table>

C. Charge-Scaling SAR ADC

The SAR ADC (blue-boxed in Figure 2) samples the differential rail-to-rail output voltages of the SC PGSA and performs binary search, based on the amount of charge stored on internal DAC nodes. Figure 8 shows a detailed diagram of the ADC composed of capacitive 12 bit charge-scaling CDACs,
clocked 2-stage comparator, bootstrapped switches for sampling and resetting functions, SAR logic and clock generation. The ADC resolution $n$ is variable between $n_{\text{min}} = 6$ bit and $n_{\text{max}} = 13$ bit.

A conversion is started by $D_{\text{soc}}$, which activates sampling signal $\phi_0$. After sampling, the comparator clock signal $D_{\text{clkComp}}$ (synchronous with $D_{\text{clk}}$) triggers the dynamic comparator $n$ times. A valid decision is flagged by asynchronous valid signal $D_{\text{valid}}$, which triggers the release of new CDAC input word $D_{p,n}$. After $n$ comparator decisions, a new $D_{\text{out}}$ is released, and $D_{\text{soc}}$ and the reset signal $D_{\text{reset}}$ are activated.

A previous version of the SAR ADC without configurable resolution, using a ladder-type CDAC, was implemented in a 22 nm fully-depleted SOI technology [8]. Since cost-efficiency is focused in this work, chip production costs are reduced by choosing a 180 nm technology. The previous approach divided the capacitor array into several subparts and used integer attenuation capacitances in between. The total capacitance and power could be reduced, and higher linearity compared to the classical split architecture could be achieved. However, the design suffered from parasitic capacitance coupling between the attenuation capacitances and substrate, when it was ported to the 180 nm technology. Therefore, linearity of the generated layouts is improved in Figure 8 by fully custom and careful routing strategy. Only one attenuation capacitor $C_{\text{atten}}$ is used to separate the array into most-significant bit (MSB) and least-significant bit (LSB) arrays. The higher total capacitance of each array reduces the effect of parasitic $C_P$. The value of $C_{\text{atten}}$ should be such that the resulting series combination with the LSB array equals the unit capacitor $C_{\text{lab}}$:

$$C_{\text{atten}} = \frac{\text{sum of LSB array capacitors}}{\text{64}}$$

The SAR ADC uses power efficient switchback switching [9] which improves the dynamic offset and the parasitic capacitance variation of the comparator by reducing the input common-mode voltage. In contrast to [9], this circuit implements a reversed scheme with a rising common-mode voltage in the first step. Hence, a N-type input can be used in the first stage of dynamic comparator, which outperformed the P-type variant.

To achieve a high level of modularity and reusability, a sophisticated calibration scheme was omitted in this design. After statistical analysis, $C_{\text{lab}} = 76 \text{fF}$ was chosen and IIP generators were used to speed up porting, however needing adaption to the older technology. The resulting $C_{\text{DAC}} \approx 2^{(n_{\text{max}}-1)}/2C_{\text{lab}}$ adds up to approximately 5 pF. The minimal power dissipation (without switching scheme) of a SAR ADC is calculated by equation (7):

$$P_{\text{min,ADC}} = C_{\text{DAC}}V_{\text{DD}}^2f_{\text{clk}}$$

For $V_{\text{DD}} = 1.8 \text{ V}$ and $f_{\text{clk}} = 140 \text{ kHz}$, $P_{\text{min,ADC}} = 2.3 \mu W$ can be calculated. The post-layout simulation results listed in Table II and the measurements show good matching to the theoretical value.

IV. RESULTS AND TESTCHIP FABRICATION

Manufacturability of the proposed AFE was verified by post-layout analysis under influence of process, voltage, temperature and mismatch variations. Simulation results for a programmed resolution of 13 bit and a sample rate of 10 kS/s are listed in Table II, compared to state-of-the-art ADC and AFE publications. The AFE is stimulated with differential 1 kHz input signals. It achieves a typical ENOB of 169.1 fJ/st. (with SC PGSA) and 30.6 fJ/st. (without SC PGSA) is obtained. Compared to AFEs targeting biomedical applications, the proposed circuit specifications meet the special demands of IoT field, and is complemented by programmable features. About 80% of the total power consumption results from the SC PGSA, which shows the importance of optimized preamplifier design.

A testchip was fabricated in a standard 180 nm low-cost SOI technology. Figure 9 shows a chip photograph and layout...
views of circuit parts. SC PGSA and SAR ADC consume areas of 0.072 mm² and 0.086 mm², respectively. Red boxes show parts, where IIP layout generators supported layout design. Ten circuit samples were characterized in laboratory. The results show good matching between measurement and simulated behavior and proof the overall working principle.

V. CONCLUSION

A configurable analog frontend ASIC, which consists of a SAR ADC and a SC PGSA in the preamplifier stage, was developed. In post-layout verification and laboratory environment, it achieves ultra-low power consumption of 10.5 µW, with medium speed and high accuracy of 12.6 bit. A new switched capacitor and switched-opamp approach reduces average current consumption and relaxes the design of the preamplifier. A testchip was fabricated. The functionality of the ASIC was already proven by experiments.

This work contributes to a modular autonomous sensor node, aimed to overcome lifetime and cost issues of present IoT hardware. It focuses on outstanding energy-efficiency, low-cost production, serving wide application standards, and reduction of costly design cycles due to semi-automatic generation of highly-reusable IP. These approaches contribute to raise acceptance of IoT systems by small and medium businesses.

TABLE II: Performance of proposed ULP AFE compared to state-of-the-art

<table>
<thead>
<tr>
<th></th>
<th>This Work</th>
<th>[5], 2017</th>
<th>[6], 2017</th>
<th>[14], 2016</th>
<th>[15], 2016</th>
<th>[9], 2013</th>
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<tr>
<td><strong>Supply (V)</strong></td>
<td>1.8</td>
<td>1.2</td>
<td>0.3</td>
<td>0.6</td>
<td>1.8</td>
<td>1.0</td>
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<tr>
<td><strong>Tech. (nm)</strong></td>
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<td>180</td>
<td>65</td>
<td>65</td>
<td>180</td>
<td>90</td>
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<td><strong>Application</strong></td>
<td>IoT</td>
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<td>Bio</td>
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<td><strong>Area (mm²)</strong></td>
<td>0.16</td>
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<td>1.0</td>
<td>1.0</td>
<td>15.6</td>
<td>10e3</td>
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<tr>
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<td>No</td>
<td>No</td>
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<td>Yes</td>
<td>No</td>
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<tr>
<td><strong>Resolution (bit)</strong></td>
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<td>8</td>
<td>10</td>
<td>8-12</td>
<td>10</td>
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<tr>
<td><strong>Power (µW)</strong></td>
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<td>0.1</td>
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<td>1.1e-3</td>
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<td>9.2</td>
<td>11.3</td>
<td>9.2</td>
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<td><strong>FoM (fJ/bit)</strong></td>
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<td><strong>Gain (dB)</strong></td>
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<tr>
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<td>5.1</td>
<td>234.3</td>
<td>N/A</td>
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³Post-layout verification results, verified in experiments

REFERENCES